

Iris HSW/BDW Schematics

Broadwell-ULT

2015-01-20

REV : A00

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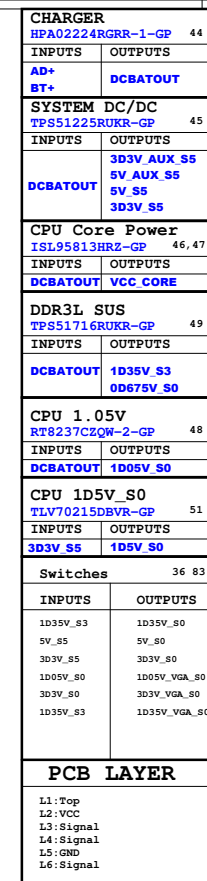
DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

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Date: Wednesday, January 21, 2015		Sheet 1 of 102			

Iris2/Tulip/VanGogh Block Diagram



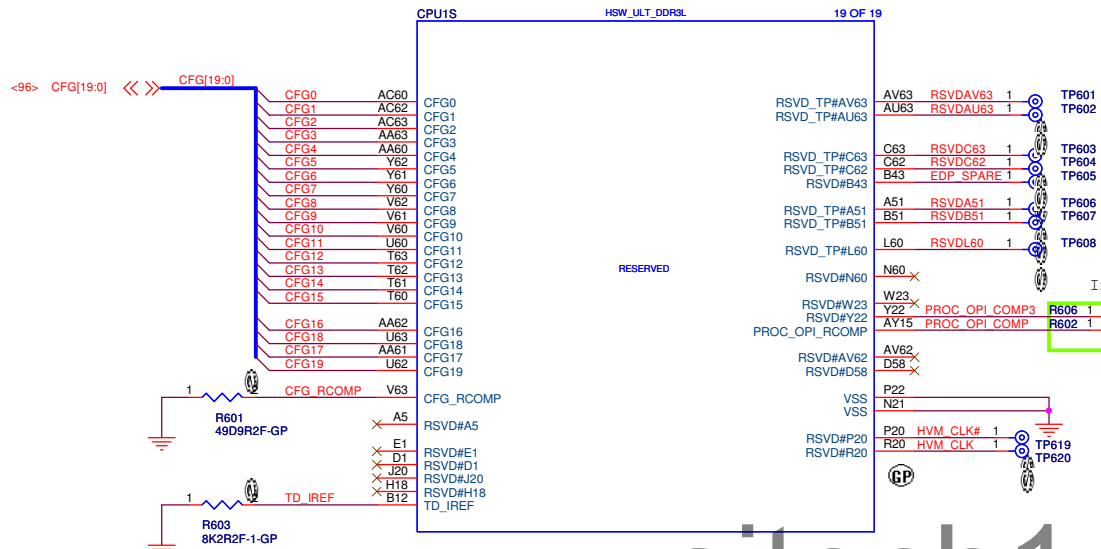
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			<i>Block Diagram</i>	
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			Date 2015-01-20	Rev A00
			Sheet 1	Total 100

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Main Func = CPU



7.4 Reserved or Unused Signals

- The following are the general types of reserved (RSVD) signals and connection guidelines:
- RSVD - these signals should not be connected
 - RSVD_TP - these signals should be routed to a test point
 - RSVD_NCTF - these signals are non-critical to function and may be left unconnected

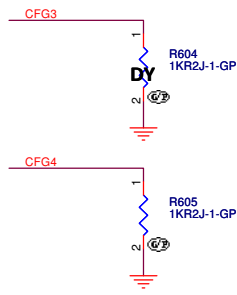
Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

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PCH strap pin:

Signal Name	Description	Direction / Buffer Type
CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate Platform Design Guide for pull-down recommendations when a logic low is desired.</p> <ul style="list-style-type: none">• CFG[2:0]: Reserved configuration lane. A test point may be placed on the board for these lanes.• CFG[3]: MSR Privacy Bit Feature<ul style="list-style-type: none">– 1 = Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting– 0 = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden• CFG[4]: eDP enable<ul style="list-style-type: none">– 1 = Disabled– 0 = Enabled• CFG[19:5]: Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

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D

C

B

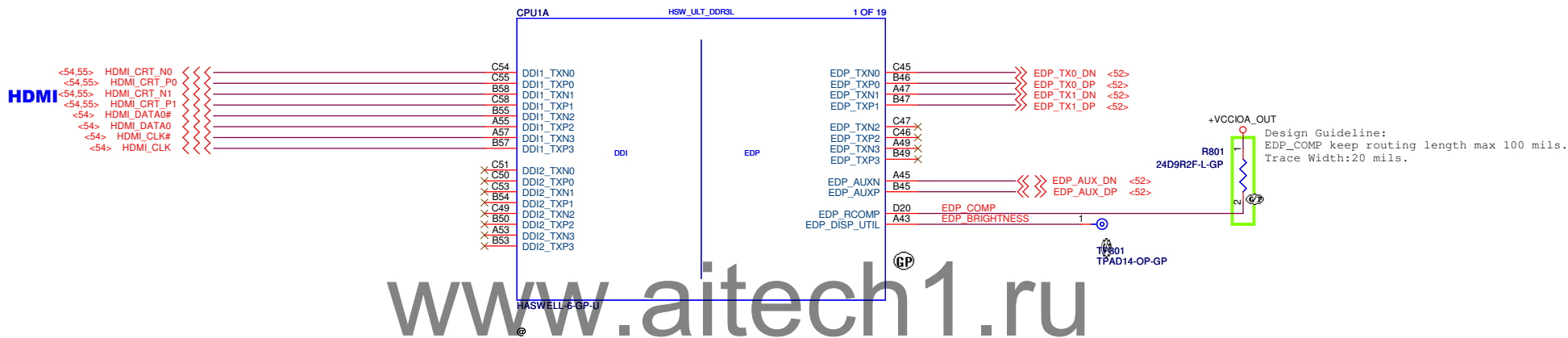
A

D

C

B

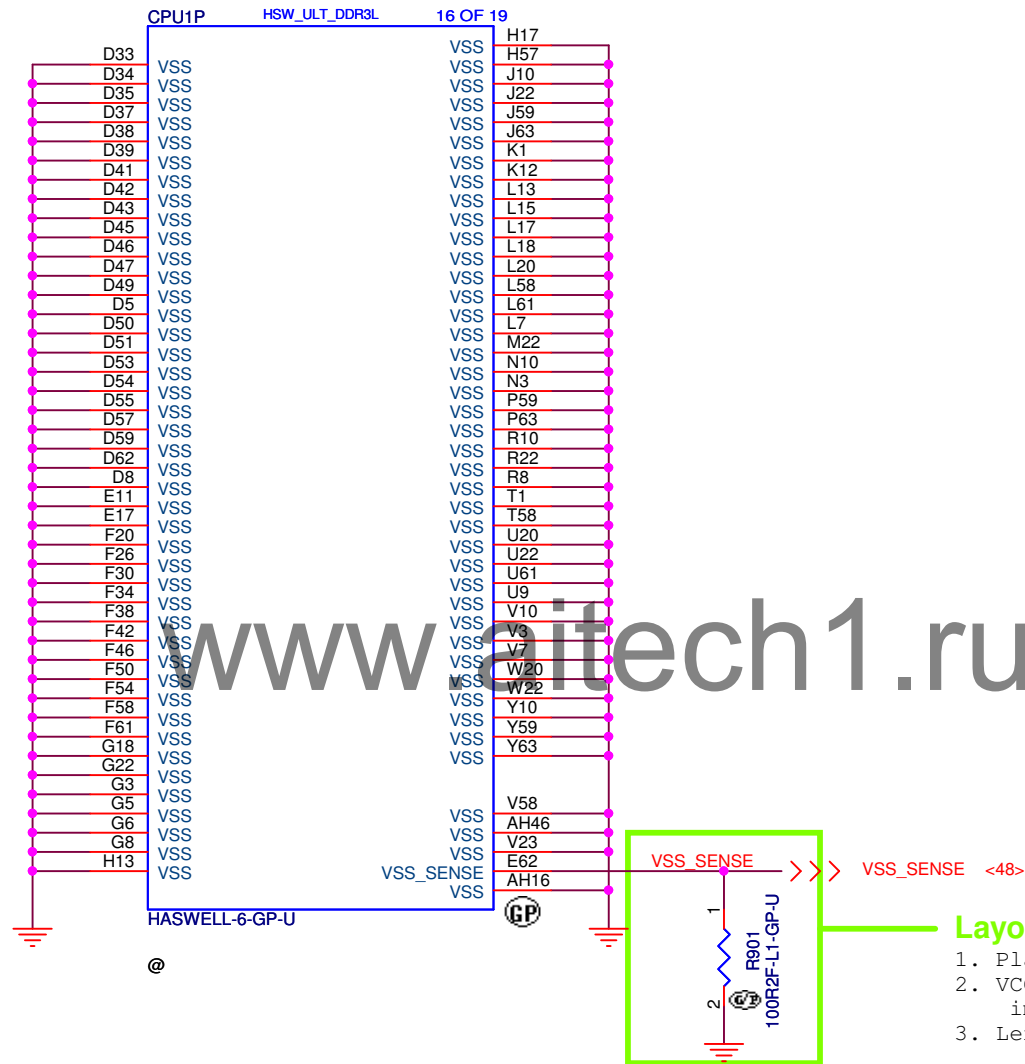
A



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Main Func = CPU

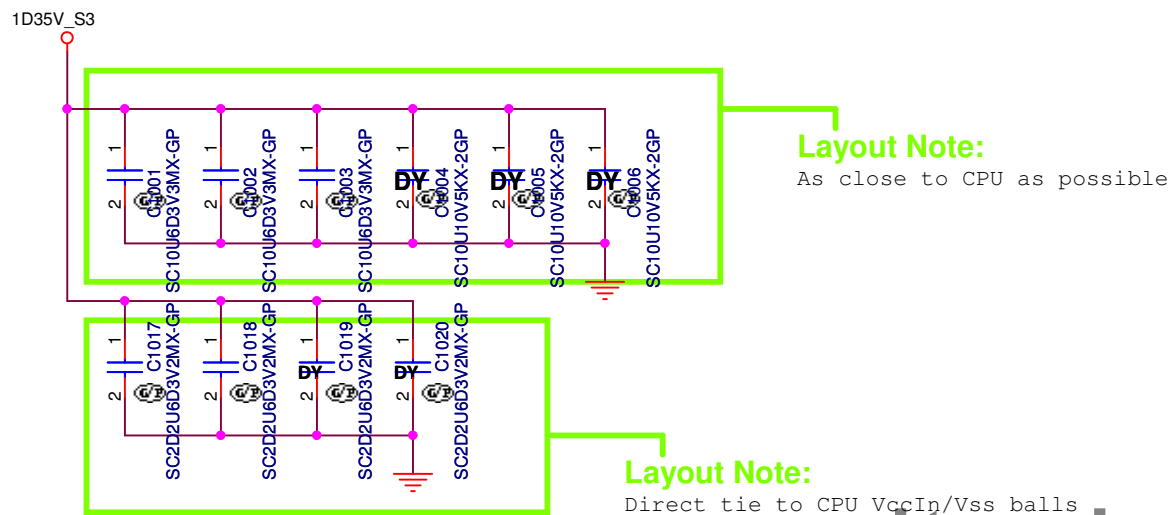


Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

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Main Func = CPU

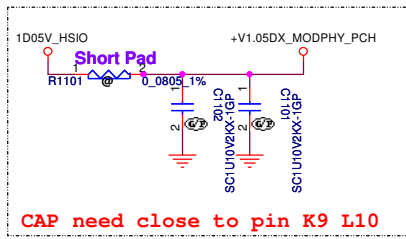


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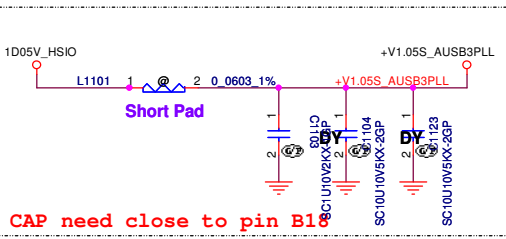
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MAX: 1.92A

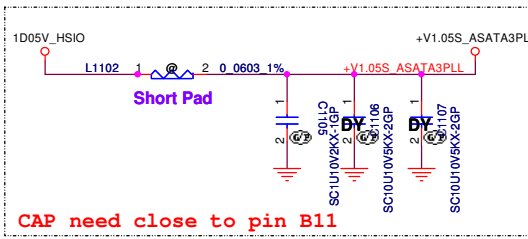
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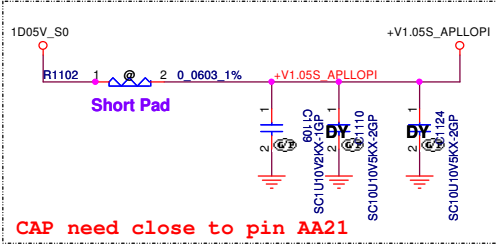
41mA



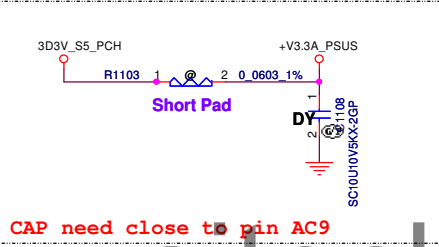
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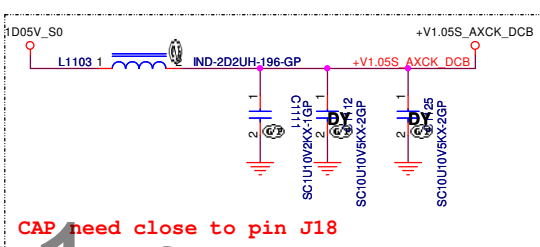
57mA



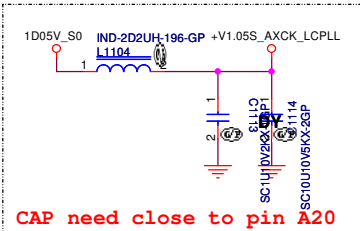
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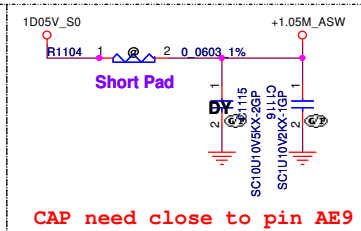
185mA



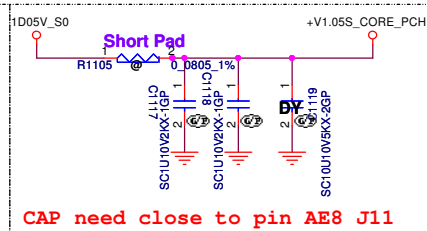
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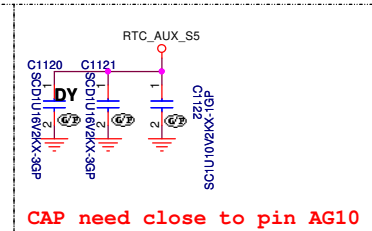
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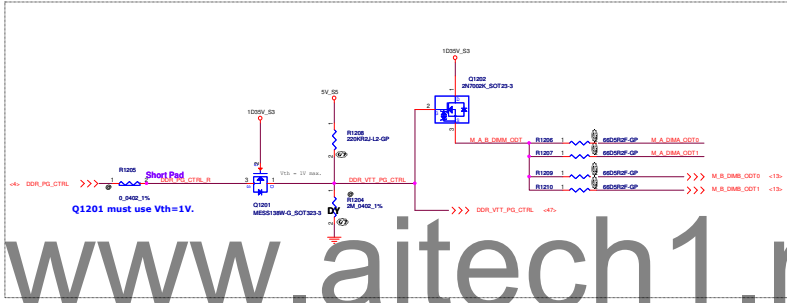


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1mA

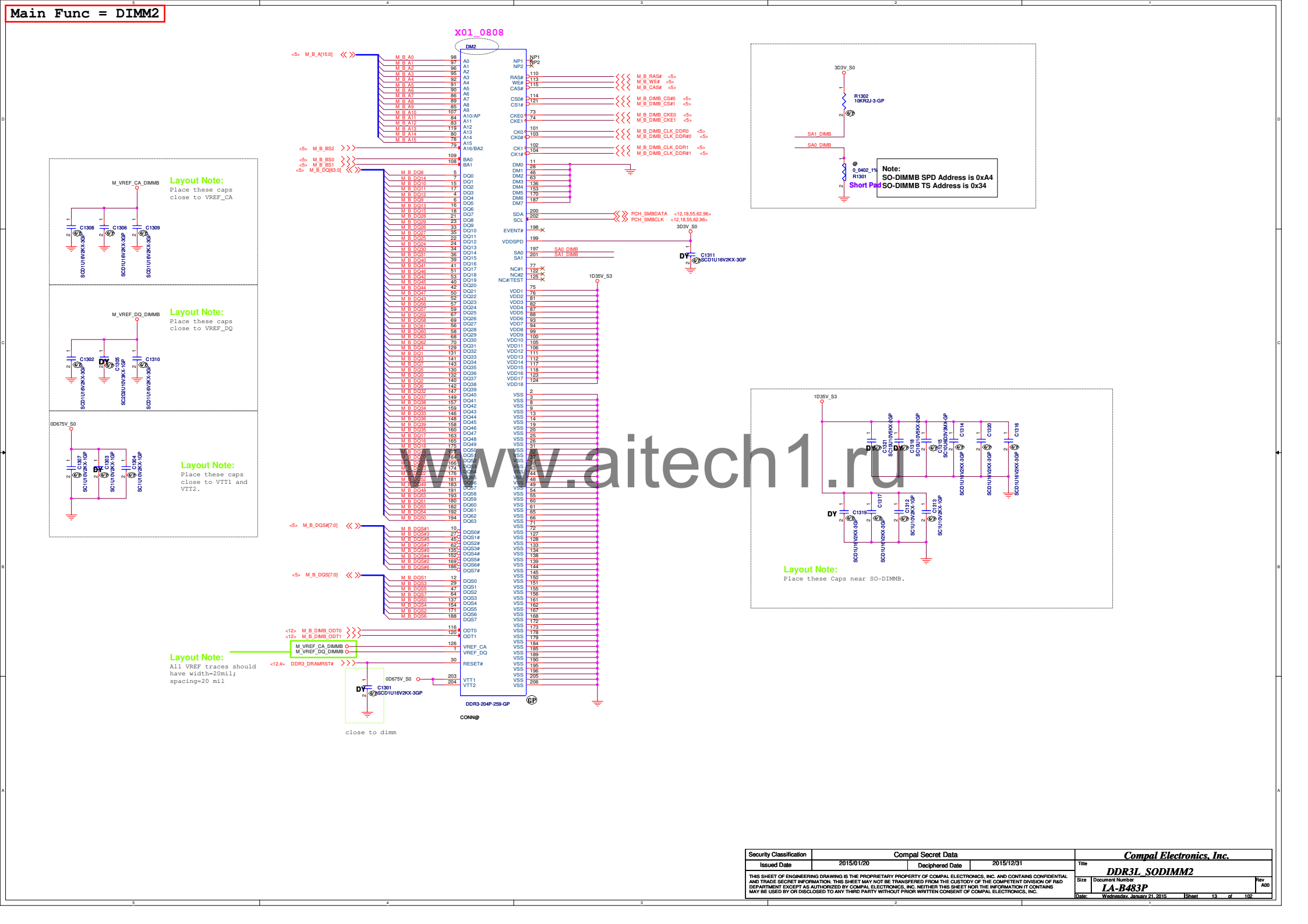
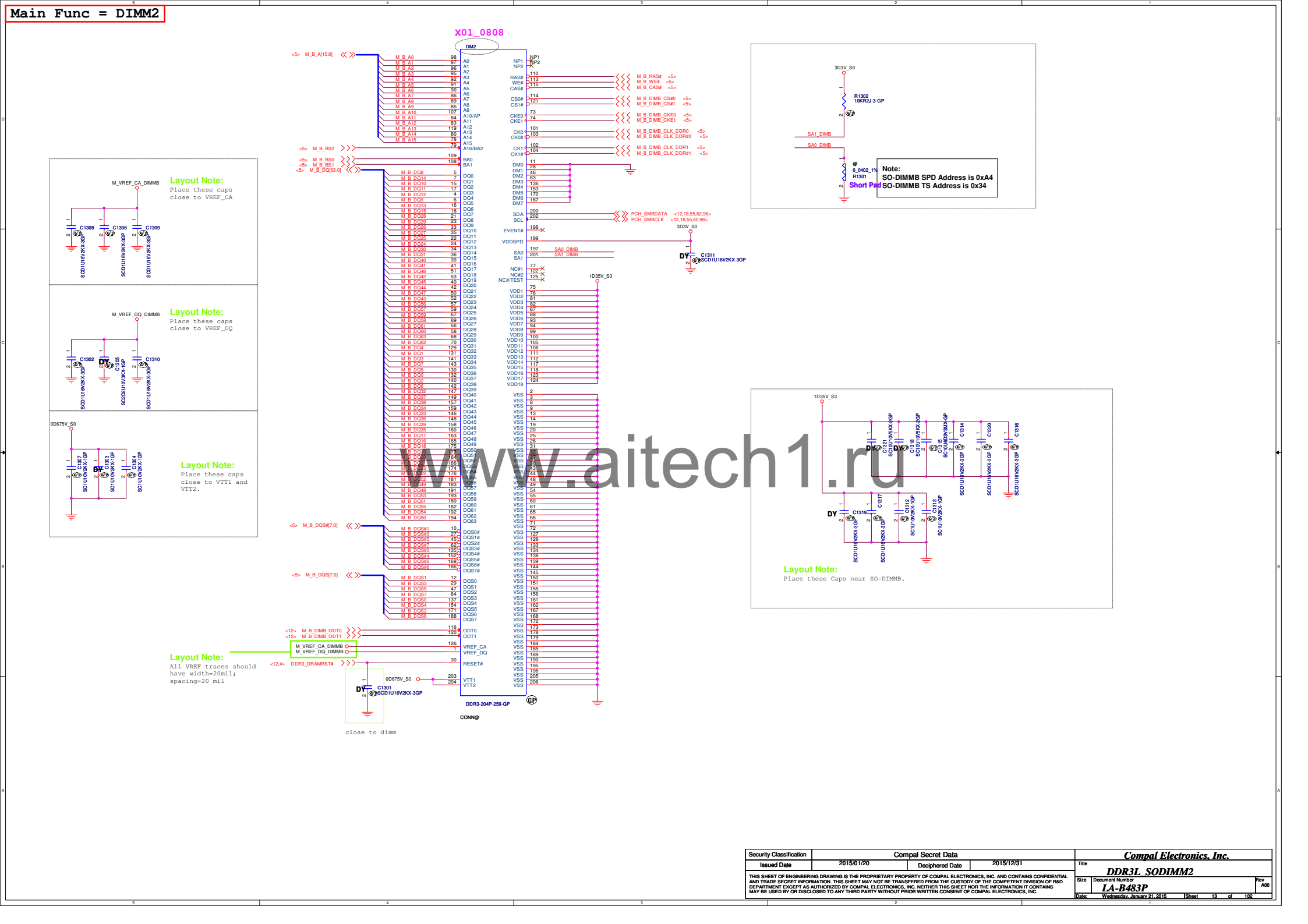




Q1201 must use V_{eh}=1V. by >>> DDR_VTT_P0_CTRL 0x75

MESS1:MMIO-0_S0T0S-0

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Main Func = DIMM2

X01_0808

Layout Note:
Place these caps close to VREF_CA

Layout Note:
Place these caps close to VREF_DQ

Layout Note:
Place these caps close to VTT1 and VTT2.

Layout Note:
All VREF traces should have width=20mil; spacing=20 mil

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

Layout Note:
Place these Caps near SO-DIMMB.

Security Classification: Compal Secret Data

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Title: DDR3L SODIMM2

Document Number: LA-B483P

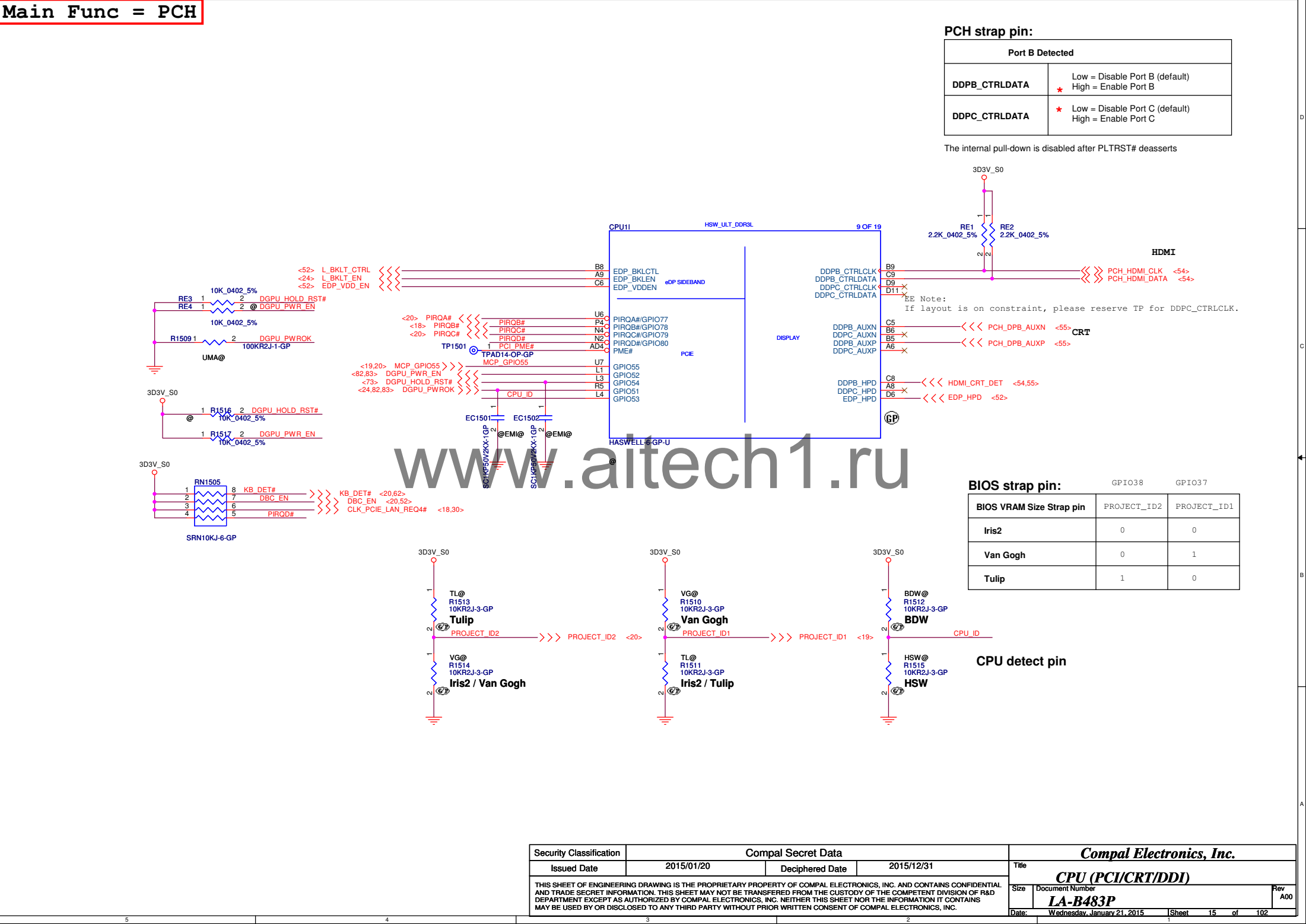
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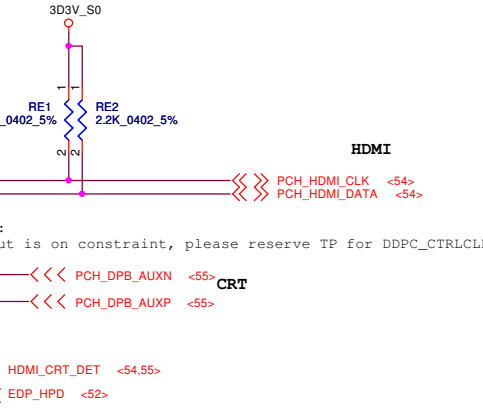
Main Func = PCH



PCH strap pin:

Port B Detected	
DDPB_CTRLCLK	Low = Disable Port B (default) ★ High = Enable Port B
DDPC_CTRLCLK	★ Low = Disable Port C (default) High = Enable Port C

The internal pull-down is disabled after PLTRST# deasserts

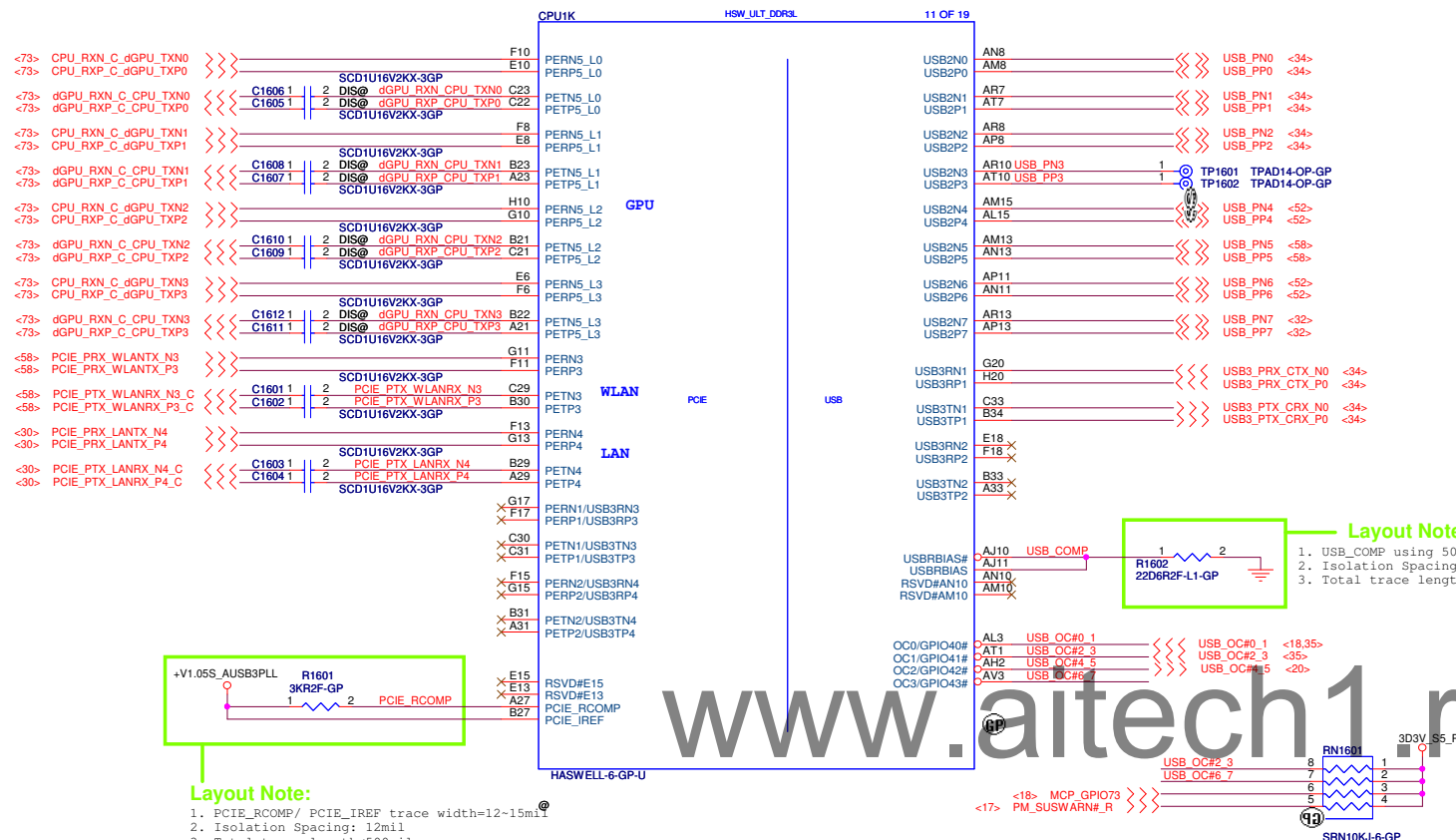


BIOS strap pin:

BIOS VRAM Size Strap pin	PROJECT_ID2	PROJECT_ID1
Iris2	0	0
Van Gogh	0	1
Tulip	1	0



Main Func = PCH



USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB2.0 Port2 (Debug Port/IOBD)
2	USB2.0 Port3 (IOBD)
3	X
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader

Layout Note:
1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN	
5 (L0~L3)	GPU	
6 (L3)	HDD	SATA0
6 (L2)	ODD	SATA1
6 (L0~L1)	N/A	

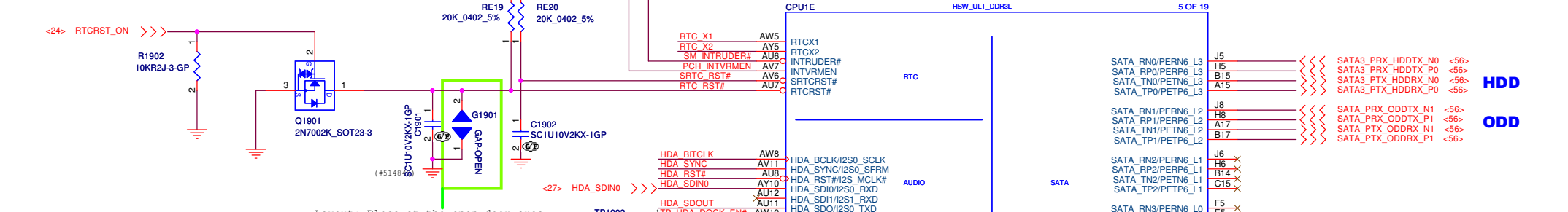
Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0	PCIe* Port 5 Lane 1	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	SATA 6Gb/s Port 3	SATA 6Gb/s Port 2	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0	PCIe* Port 5 Lane 1	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	PCIe* Port 6 Lane 0	PCIe* Port 6 Lane 1	PCIe* Port 6 Lane 2	PCIe* Port 6 Lane 3

Main Func = PCH

PCH strap pin:

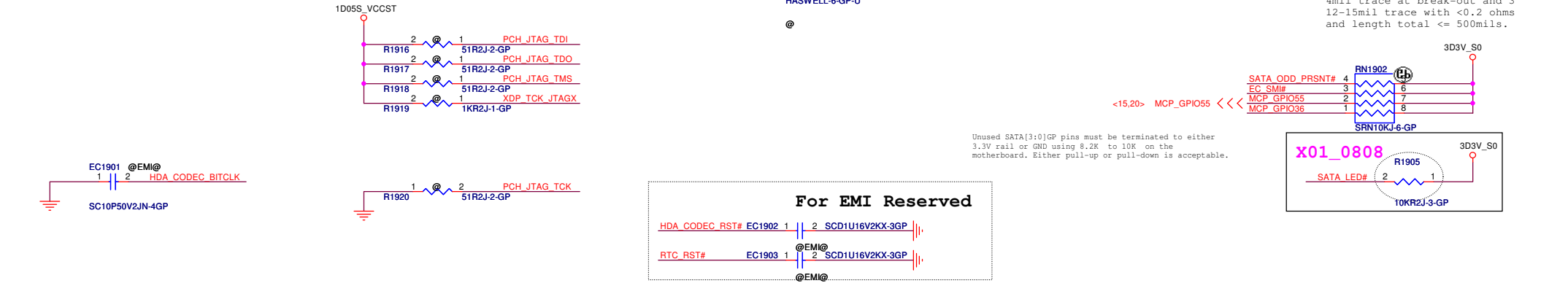
Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs★



PCH strap pin:

Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default ★ High = Enable

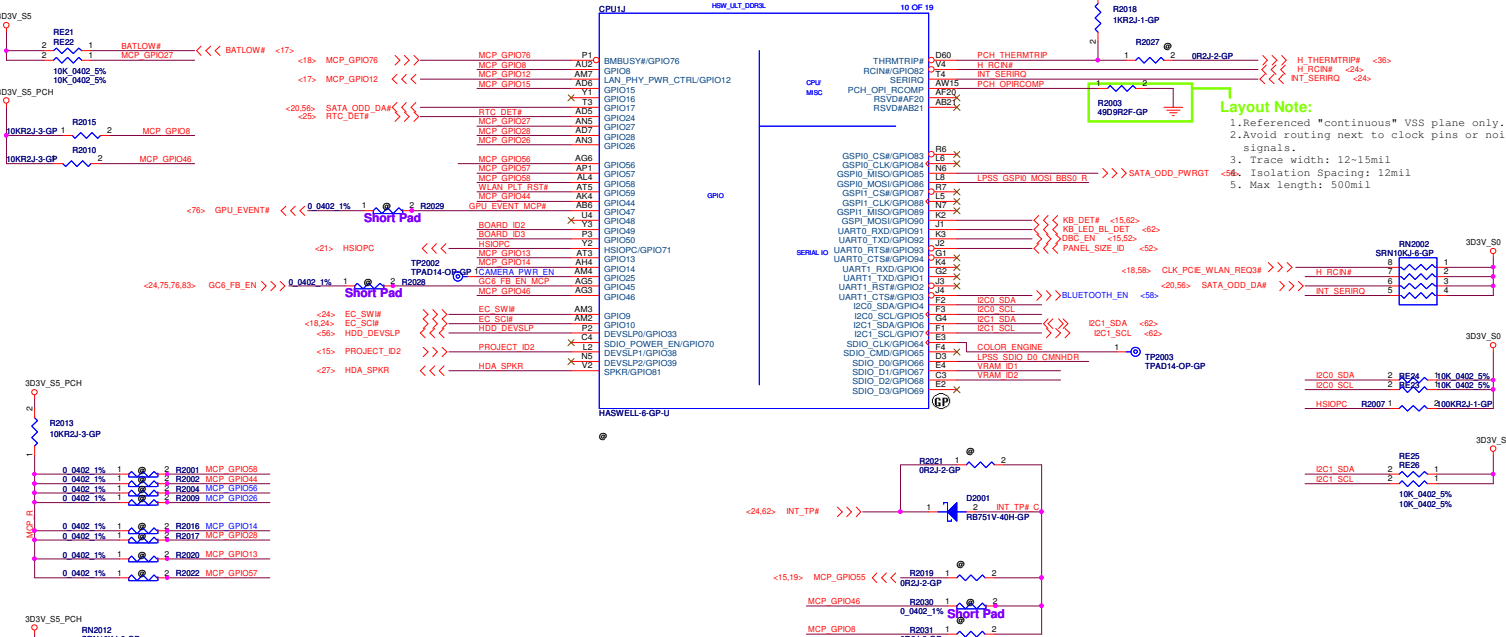
The internal pull-down is disabled after PLTRST# deasserts



Layout Note:
4mil trace at break-out and 3
12-15mil trace with <0.2 ohms
and length total <= 500mils.

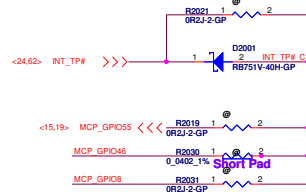
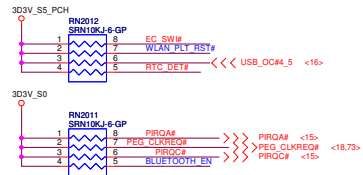
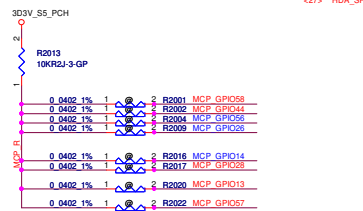
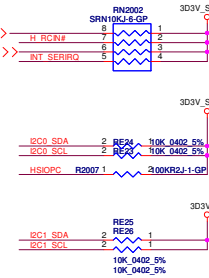
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Main Func = PCH

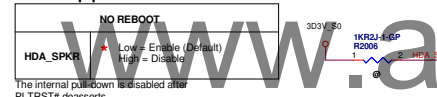


Layout Note:

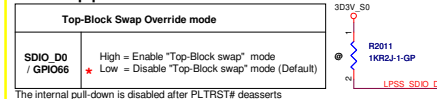
1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil



PCH strap pin:

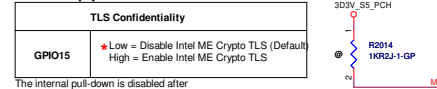


PCH strap pin:



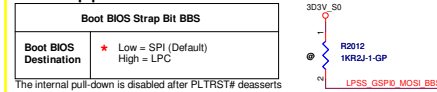
Need SW double confirm if that's needed Top-Block swap

PCH strap pin:



The internal pull-down is disabled after RSMRST# deasserts.

PCH strap pin:



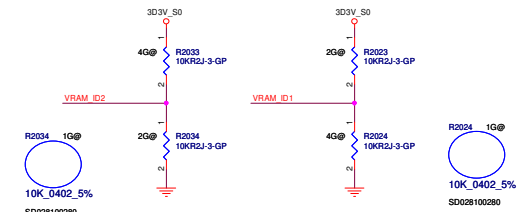
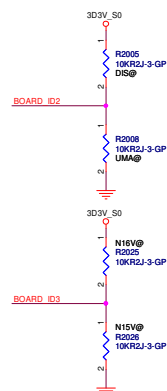
Need double confirm, GPIO table set to GPI if that's needed PH or PL

BIOS strap pin:

BIOS UMA/DIS Strap pin	BOARD _{max} ID2
UMA	0
DIS	1

BIOS strap pin:

BIOS UMA/DIS Strap pin	BOARD_ID3
N15V-GM	0
N16V-GM	1

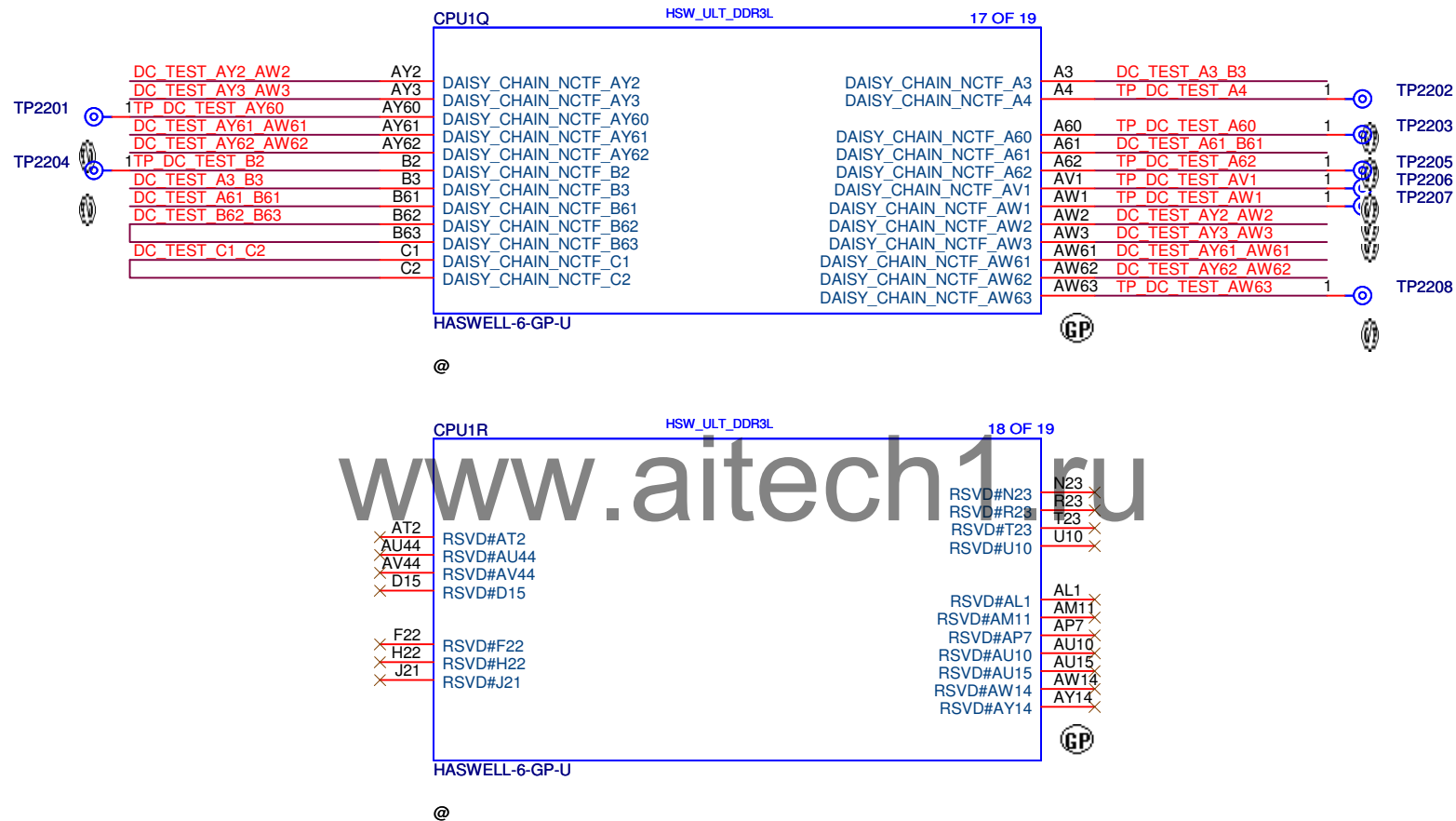


BIOS strap pin:

BIOS VRAM Size Strap pin	VRAM_ID2	VRAM_ID1
1G	0	0
2G	0	1
4G	1	0

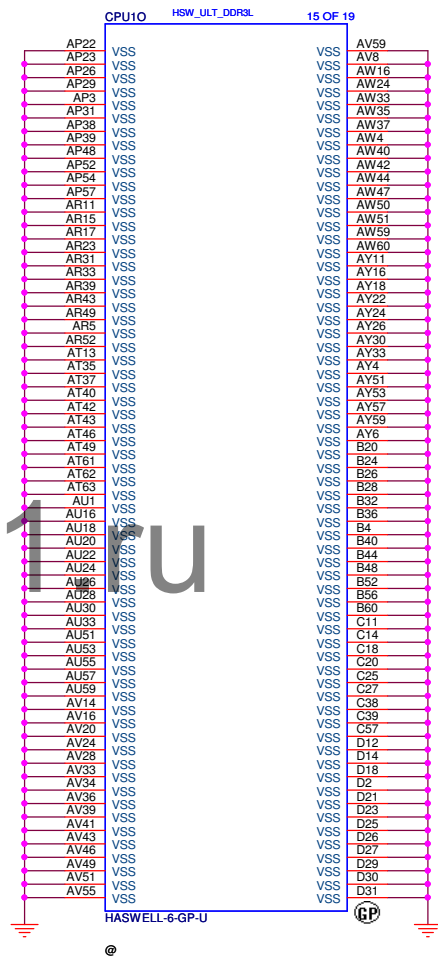
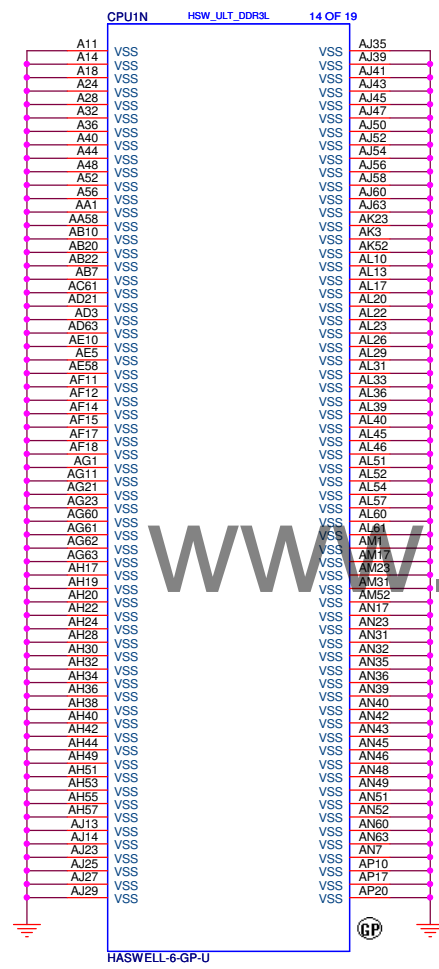
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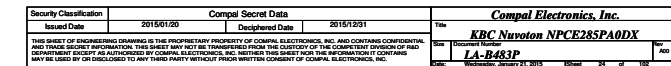
Main Func = PCH



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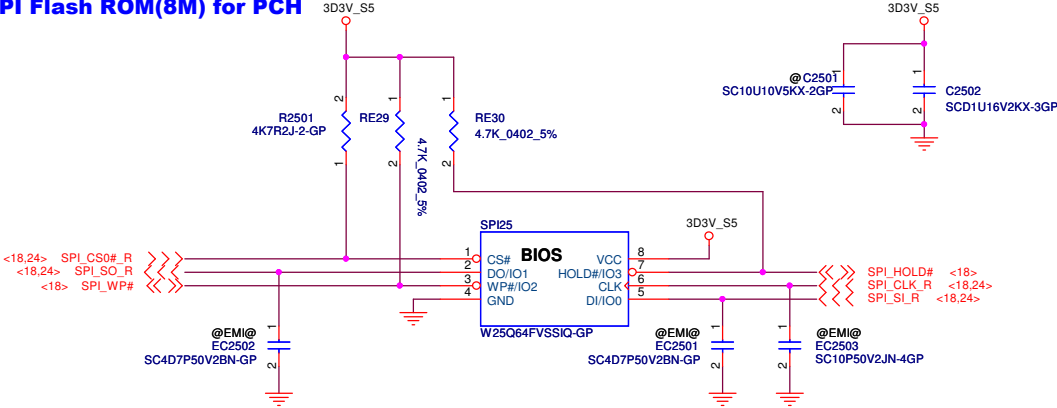
Main Func = PCH





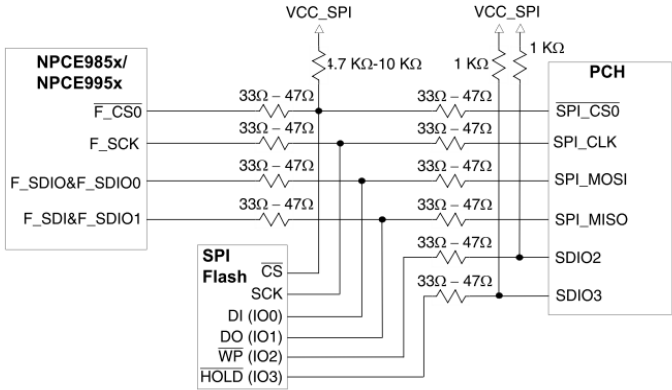
Main Func = SPI Flash

SPI Flash ROM(8M) for PCH



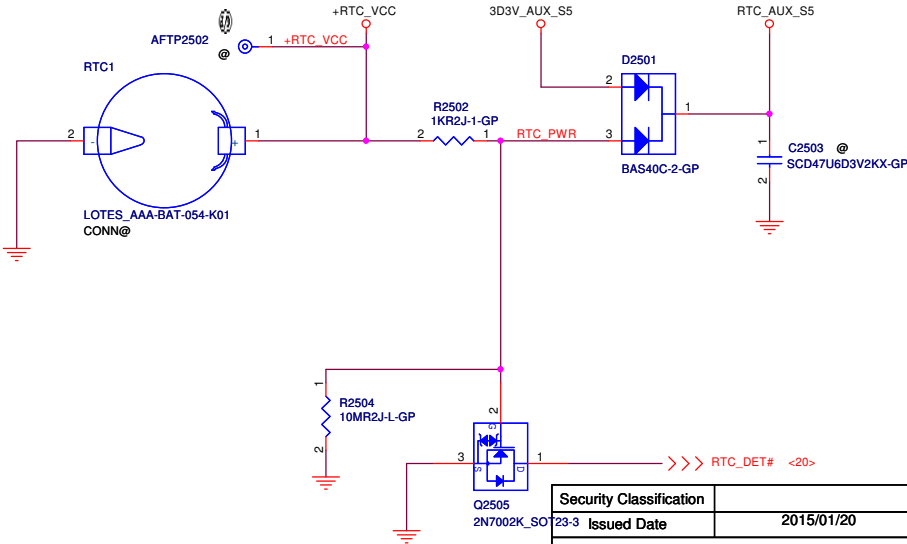
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	o	o
72.25647.00A	o	o
072.25B64.0001	o	o

Single SPI shared flash connection (SPI Quad I/O mode)

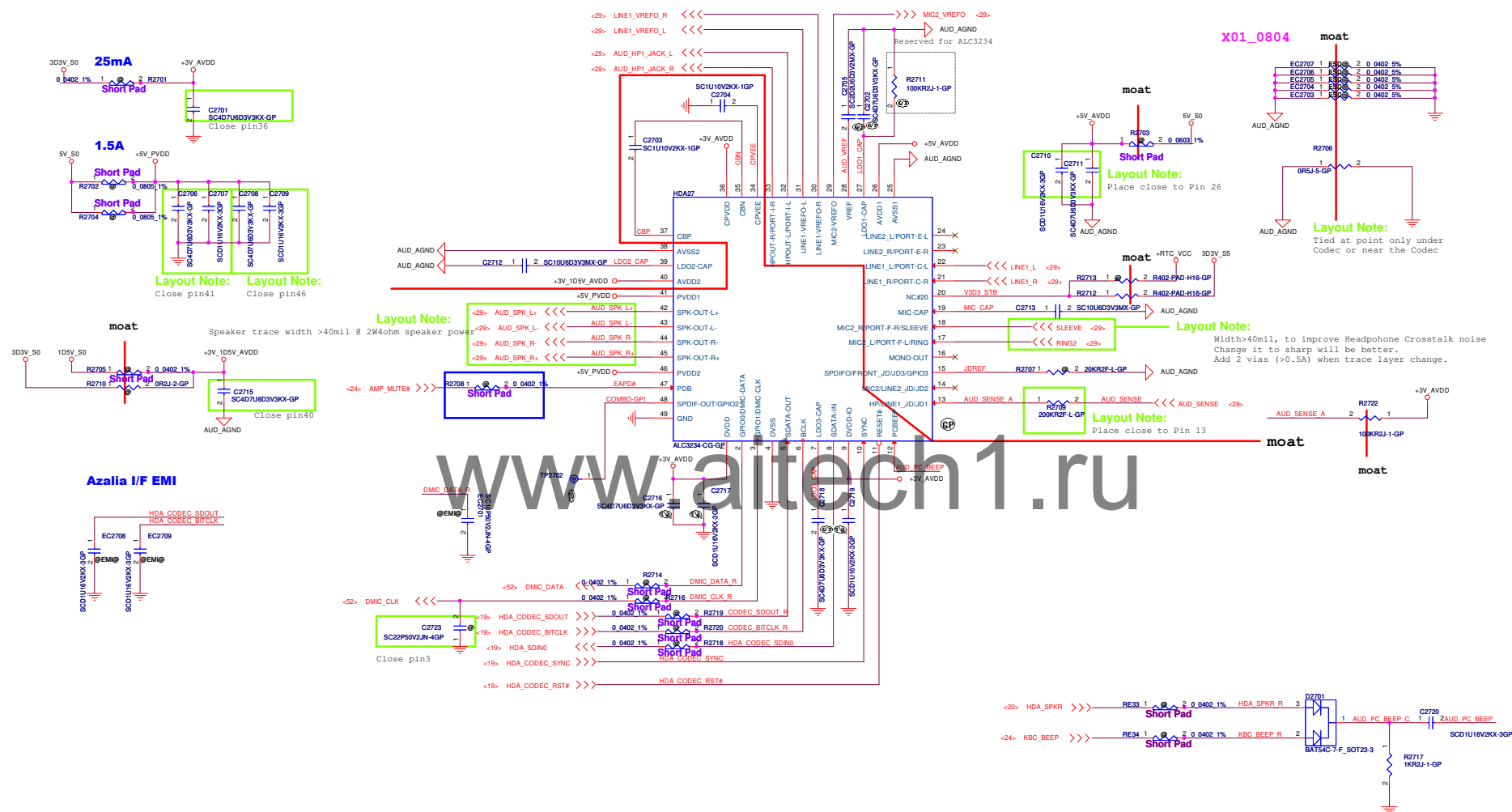



Refer to "NCPE985x/ NPCE995x board design reference guide"

Main Func = RTC



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Date				Wednesday, January 21, 2015				Sheet 25 of 102			
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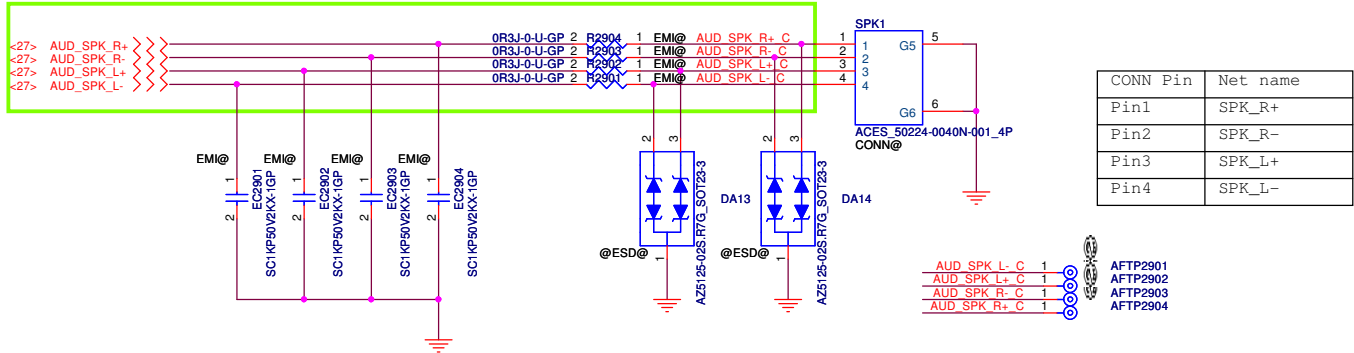
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2015/01/20	Deciphered Date	2015/12/31	Reserved		
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				Size	LA-B483P	A00
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Main Func = Audio

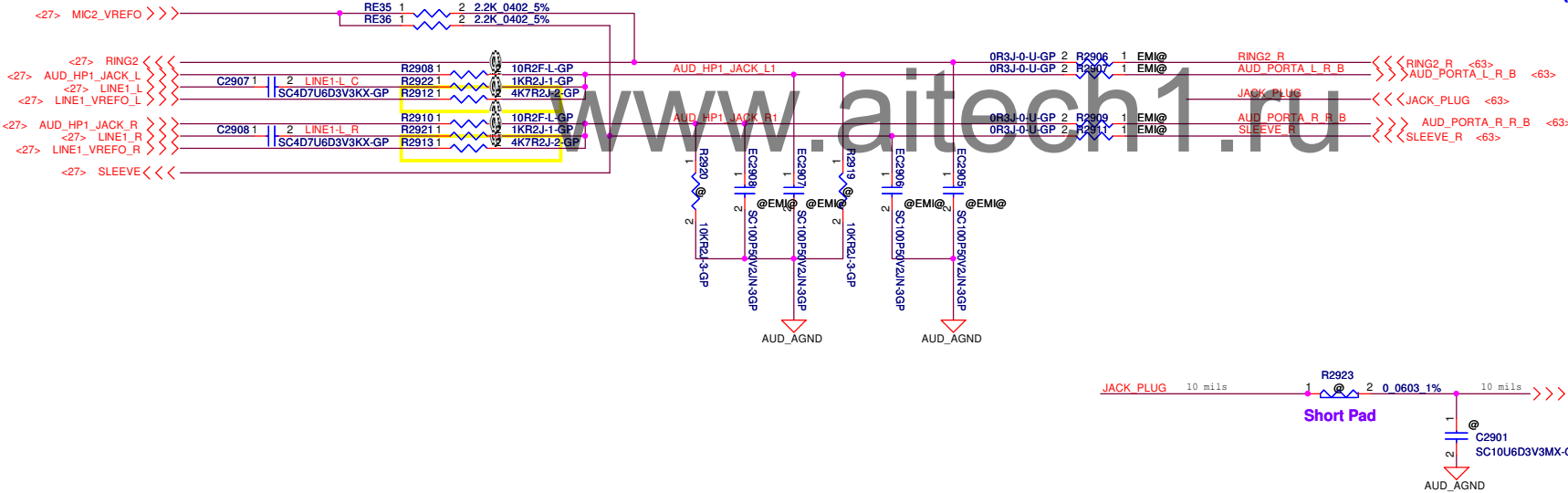
Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

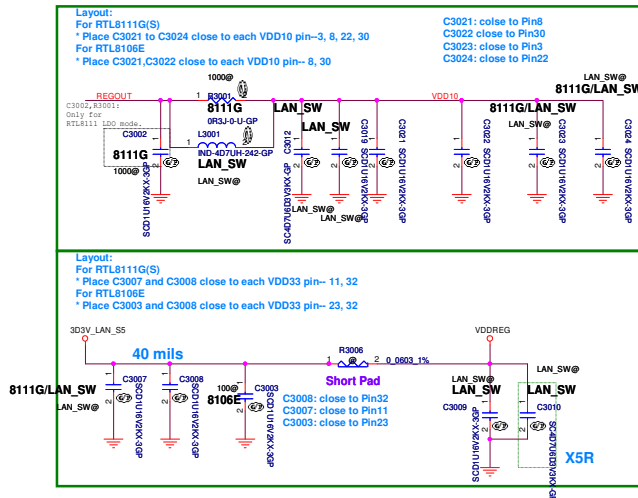


Universal Jack (Moved to I/O Board)

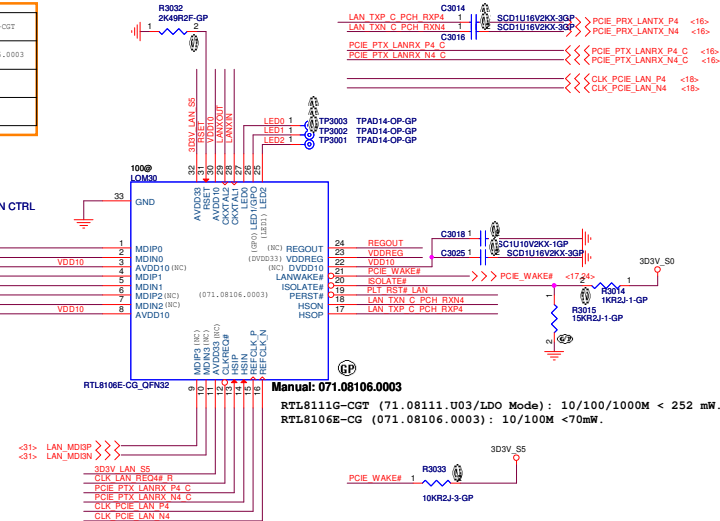
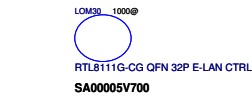


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Issued Date		2015/01/20		Title	
		Deciphered Date		SPEAKER/AUDIO JACK	
				Size	
				Document Number	
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				A00	
				Date	
				Wednesday, January 21, 2015	
				Sheet	
				29 of 102	

LAN CHIP (10/100/1000M & 10/100M co-lay)

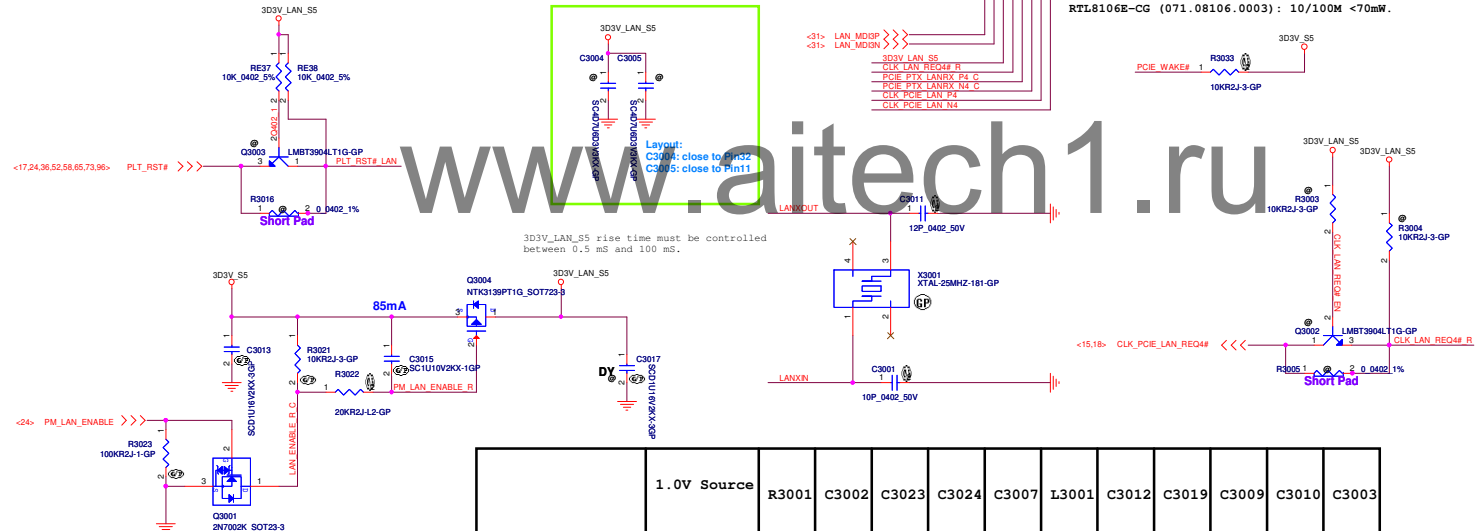


RTL8111GUS-CG	RTL8111G-CGT	RTL8106EUS-CG	RTL8106E-CGT
71.08111.W03	71.08111.003	71.08106.003	071.08106.0003
SWR mode	LDO mode	SWR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M



Manual: 071.08106.0003

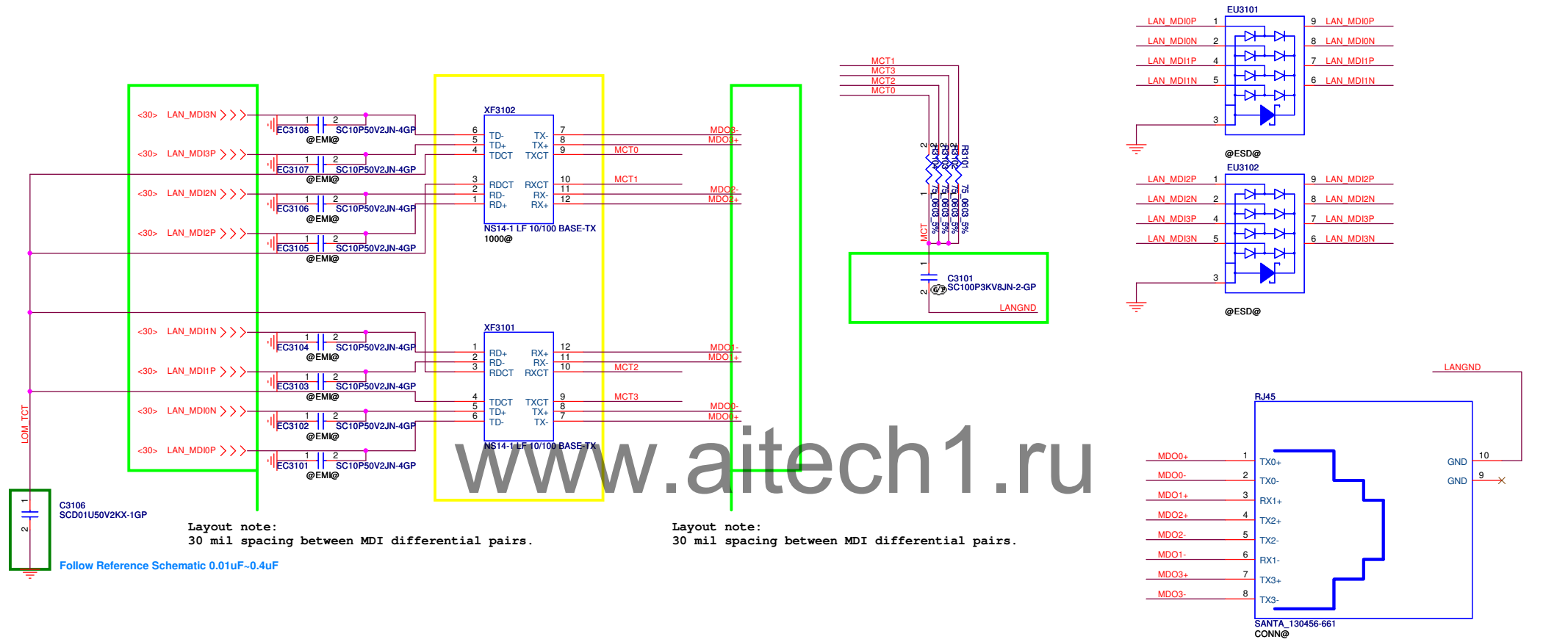
RTL8111G-CGT (71.08111.U03/LDO Mode): 10/100/1000M < 252 mW.
RTL8106E-CG (071.08106.0003): 10/100M <70mW.

[illegible]

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			Size	Document Number
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Main Func = LAN

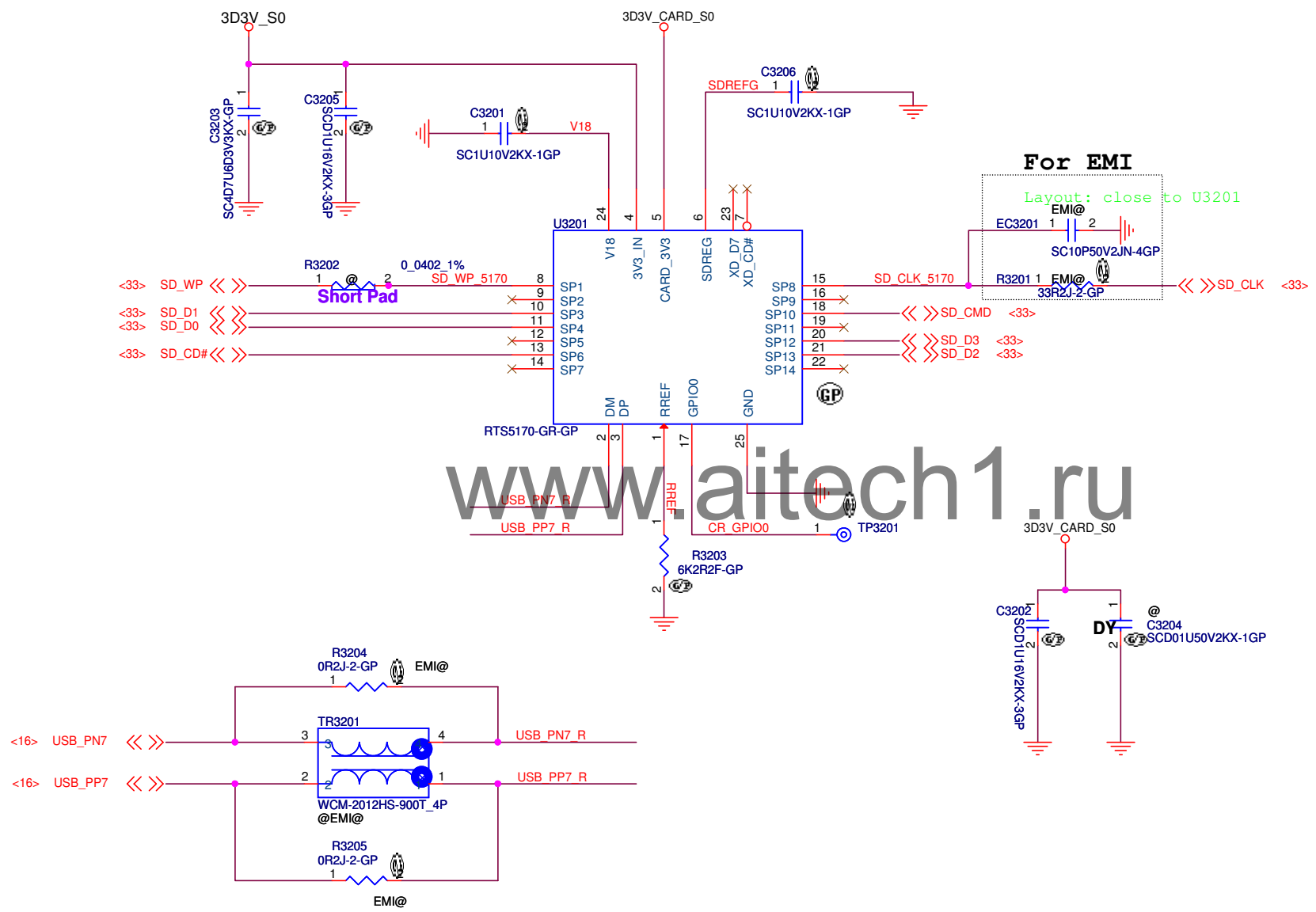
LAN TransFormer (10/100/1000M & 10/100M co-lay)



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				Date	Wednesday, January 21, 2015
				Sheet	31 of 102

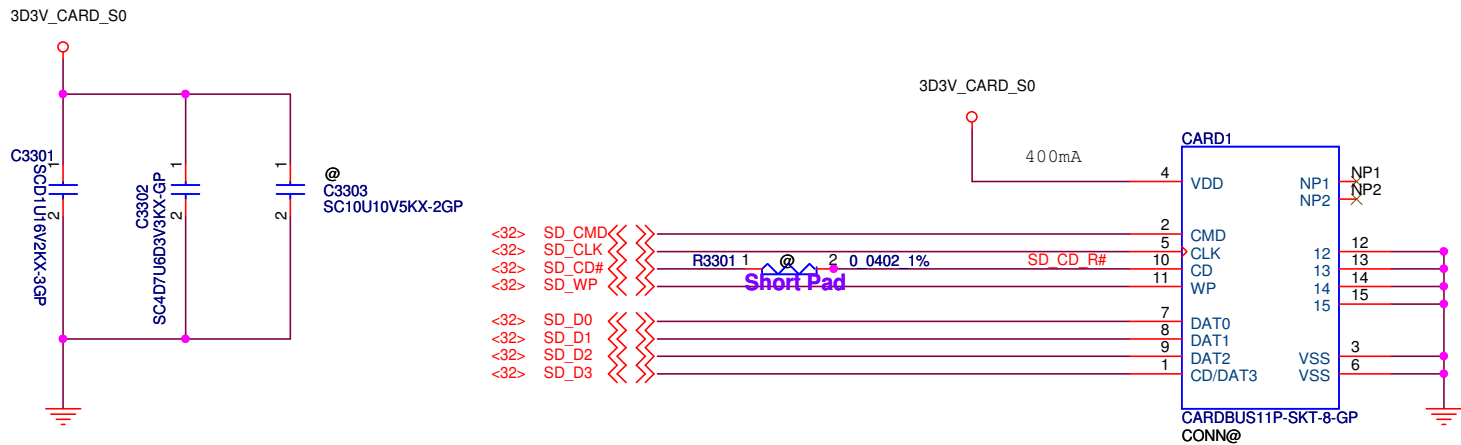
Main Func = Card Reader

The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA

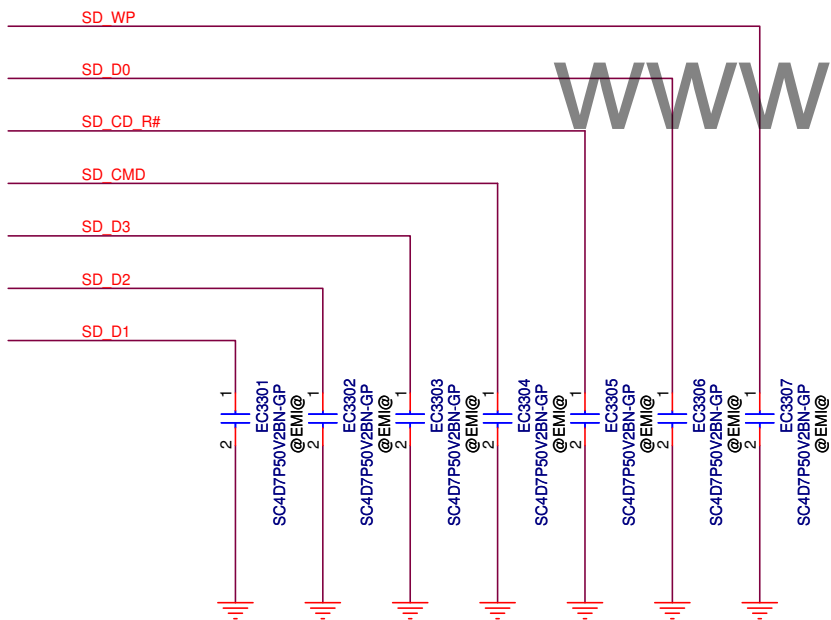


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				Size	Document Number
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Main Func = Card Reader



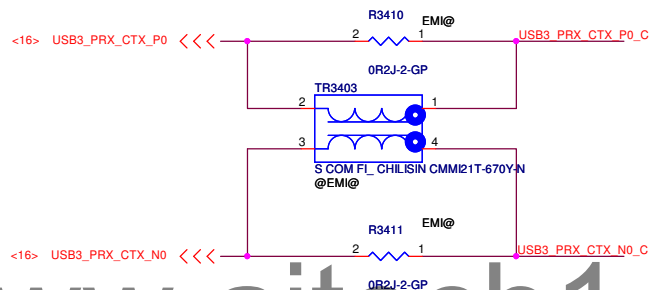
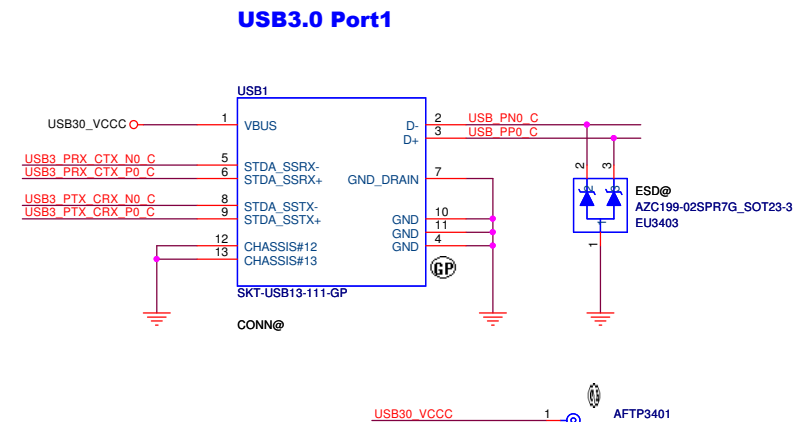
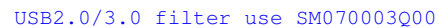
For EMI Reserved



SD_CMD	1	AFTP3302
SD_CLK	1	AFTP3303
SD_CD_R#	1	TP3304
SD_WP	1	TP3305
SD_D0	1	AFTP3306
SD_D1	1	TP3307
SD_D2	1	TP3308
SD_D3	1	TP3309
3D3V_CARD_S0	1	TP3310

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Size		Document Number			Rev
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USB2.0 Port2 and USB2.0 Port3 are on IOBD



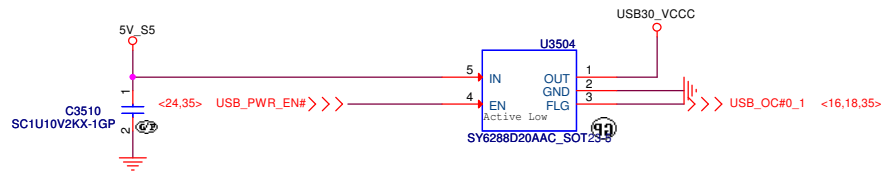
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[illegible]

Layout Note:
Close to CON1

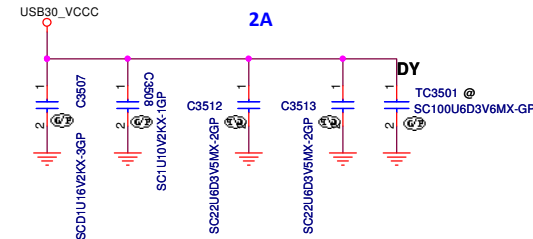
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Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title USB3.0 CONN		
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Main Func = USB3.0 Port1



USB3.0 Port1

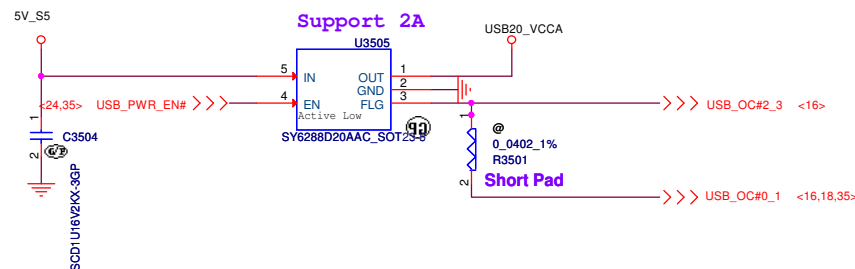
Layout Note: Close USB1



Main Func = USB2.0 Port2

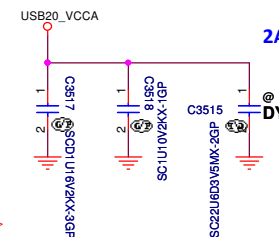
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Main Func = USB2.0 Port3



USB2.0 Port3 (IO Board)

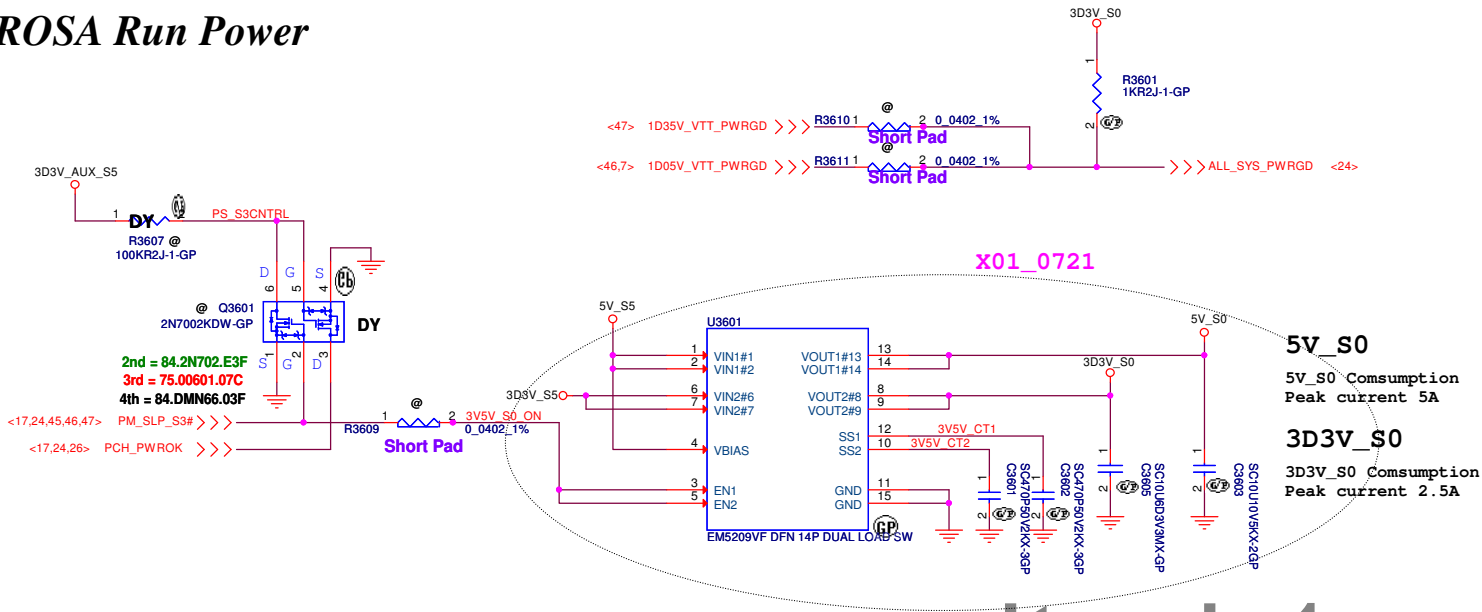
Layout Note: Close CON1



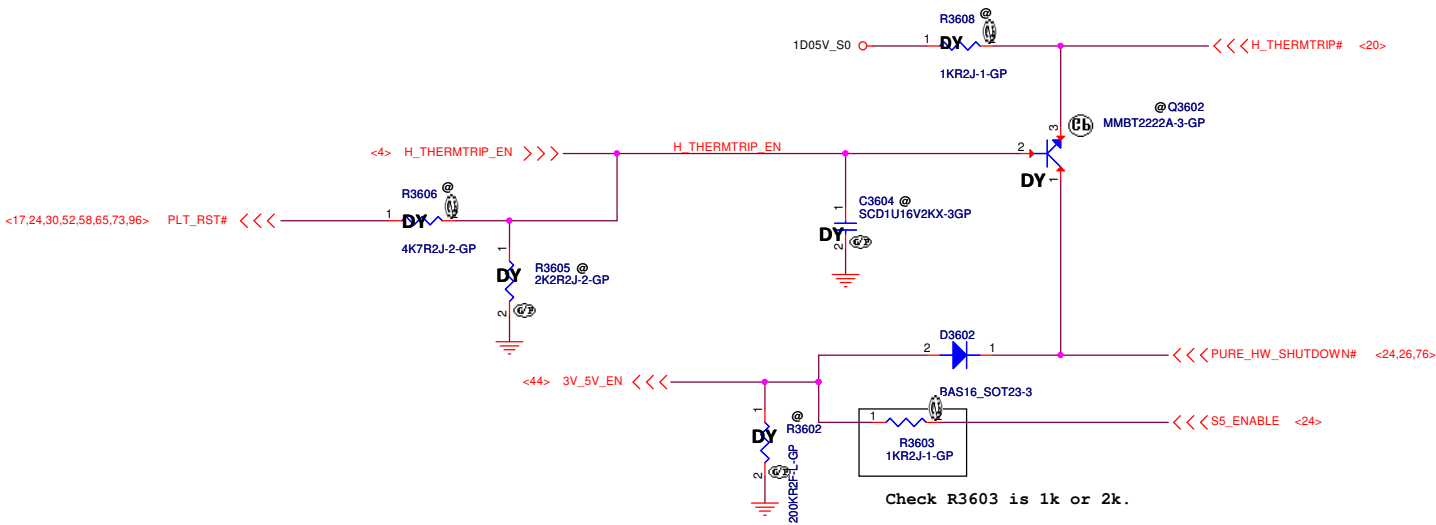
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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Power Good

ROSA Run Power

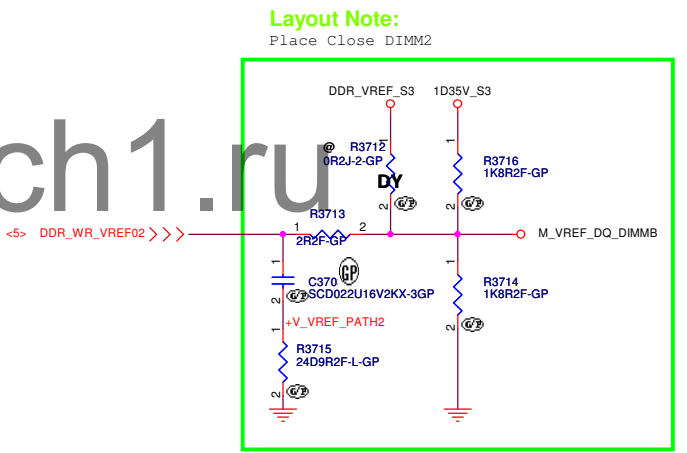
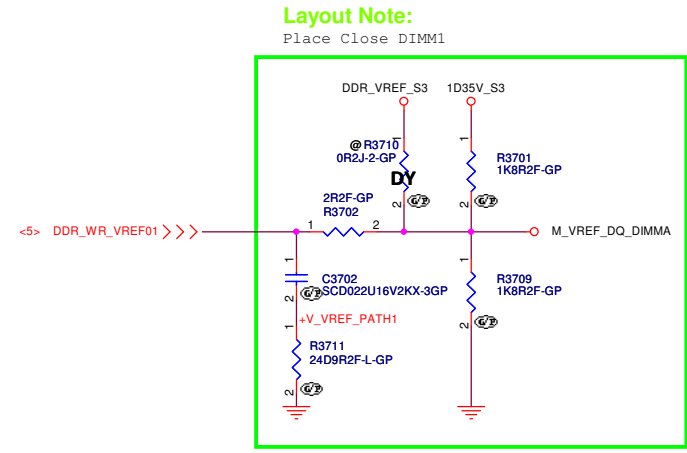
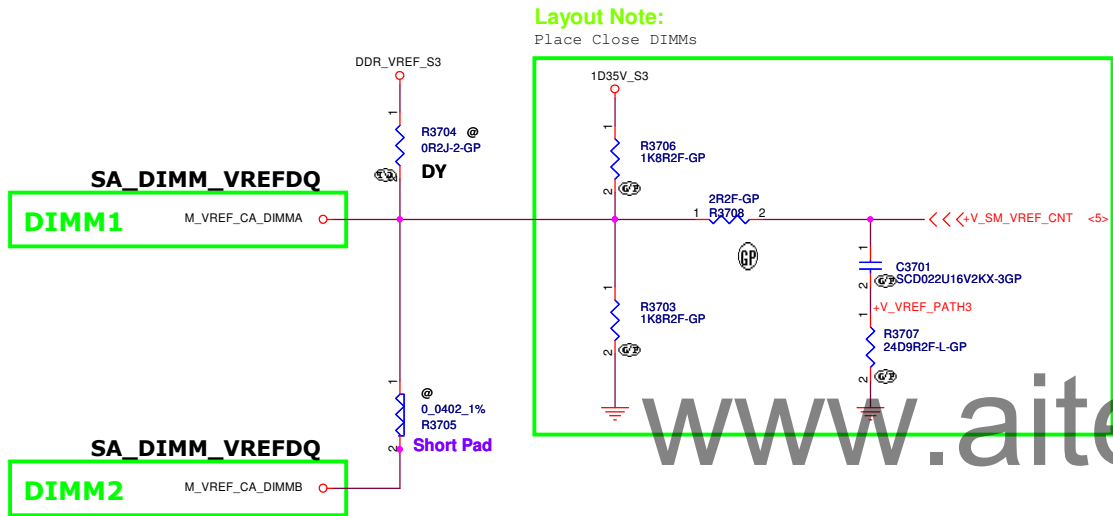


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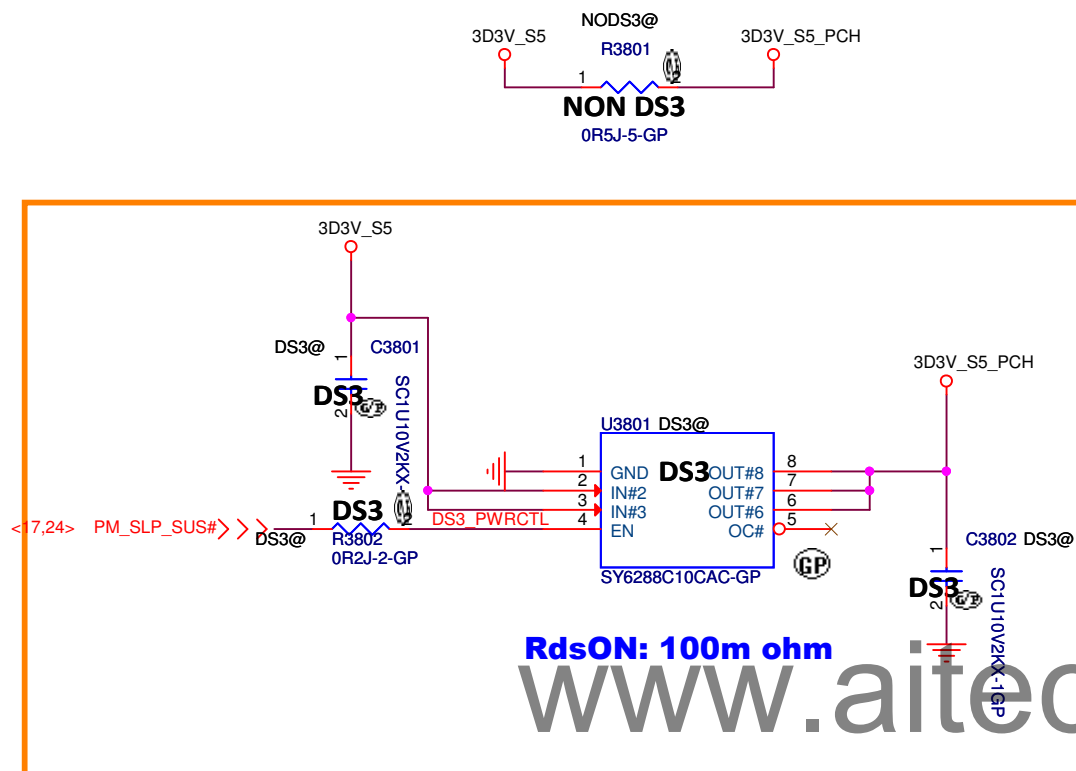


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Main Func = DIMM1
Main Func = DIMM2



Main Func = Power Plane & Sequence



DS3

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		Size		Document Number		Rev		A00	
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		Date:		Wednesday, January 21, 2015		Sheet		39 of 102	

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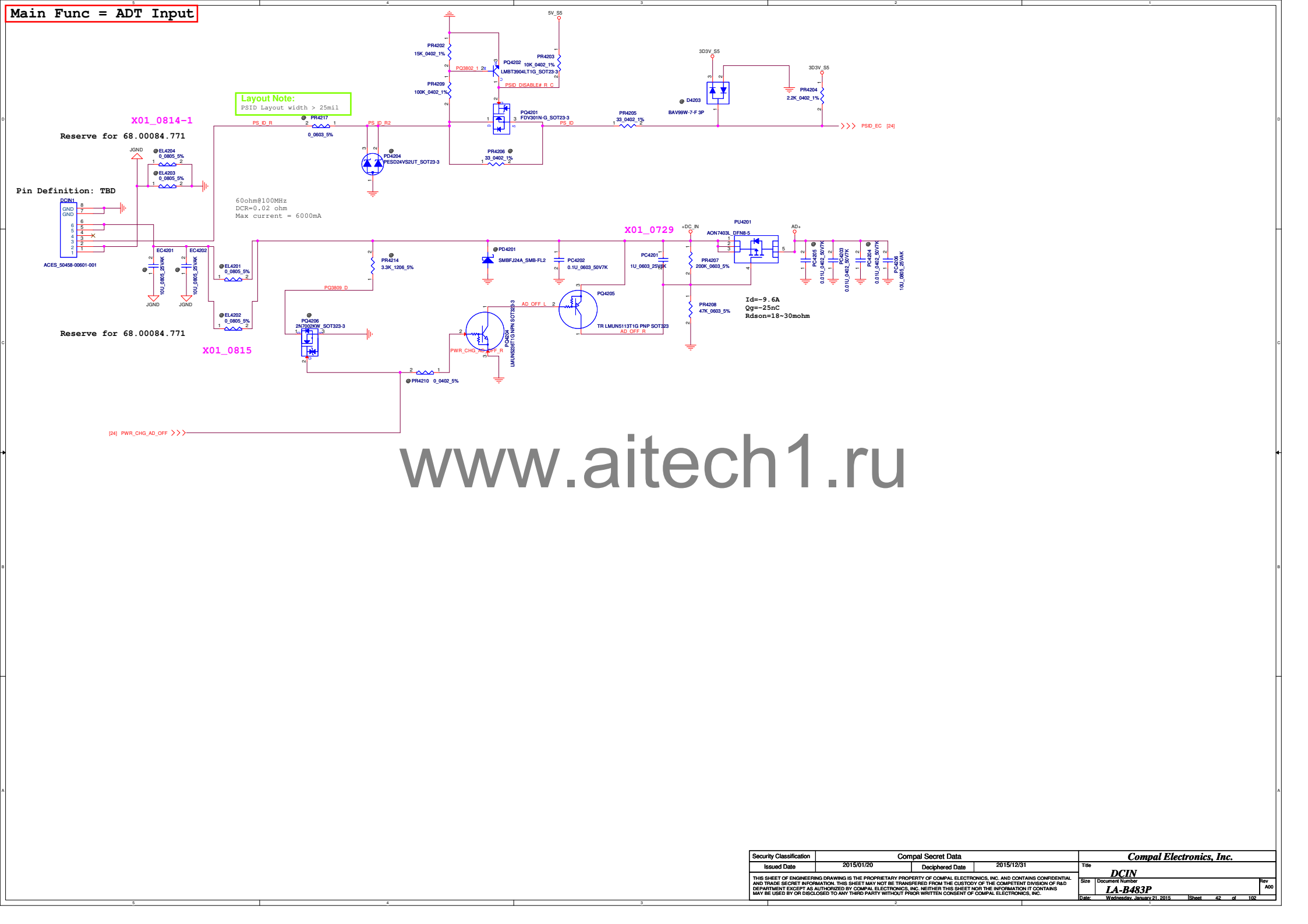
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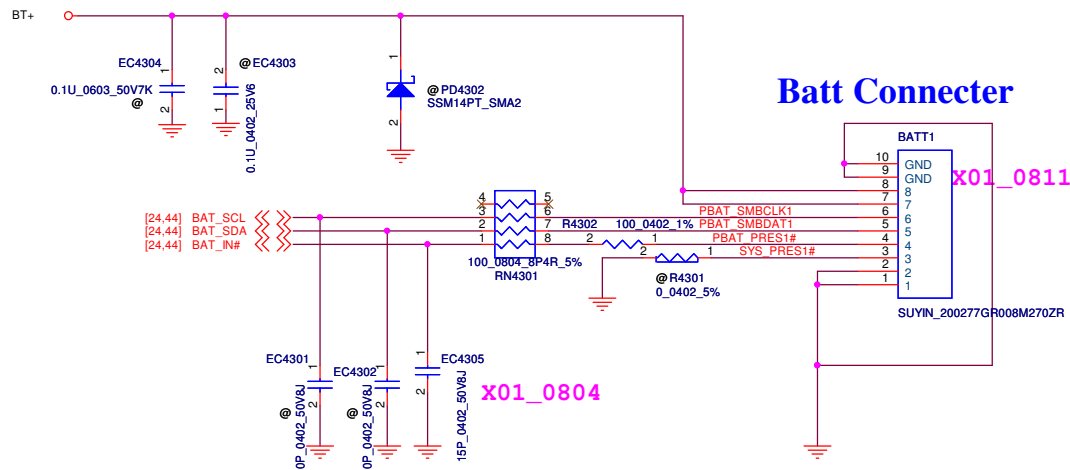
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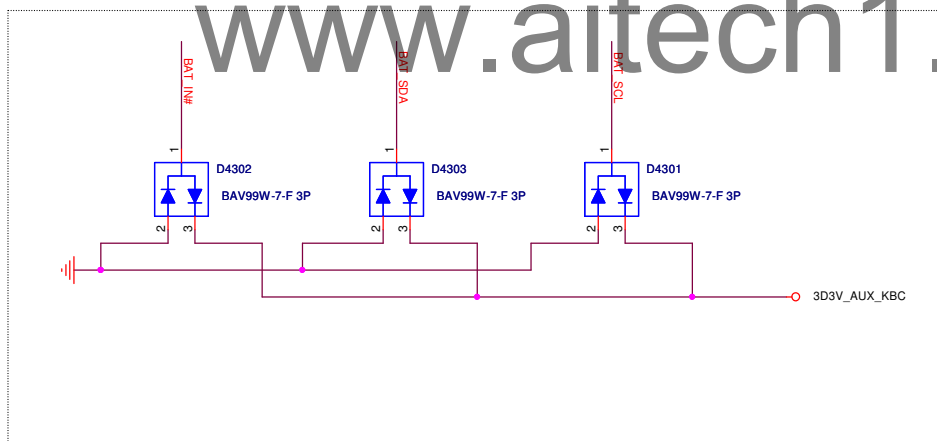
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Issued Date		2015/01/20		Deciphered Date		2015/12/31		Title			
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						Size		Document Number		Rev	
								LA-B483P		A00	
						Date:		Wednesday, January 21, 2015		Sheet 41 of 102	



Main Func = M-BAT Input

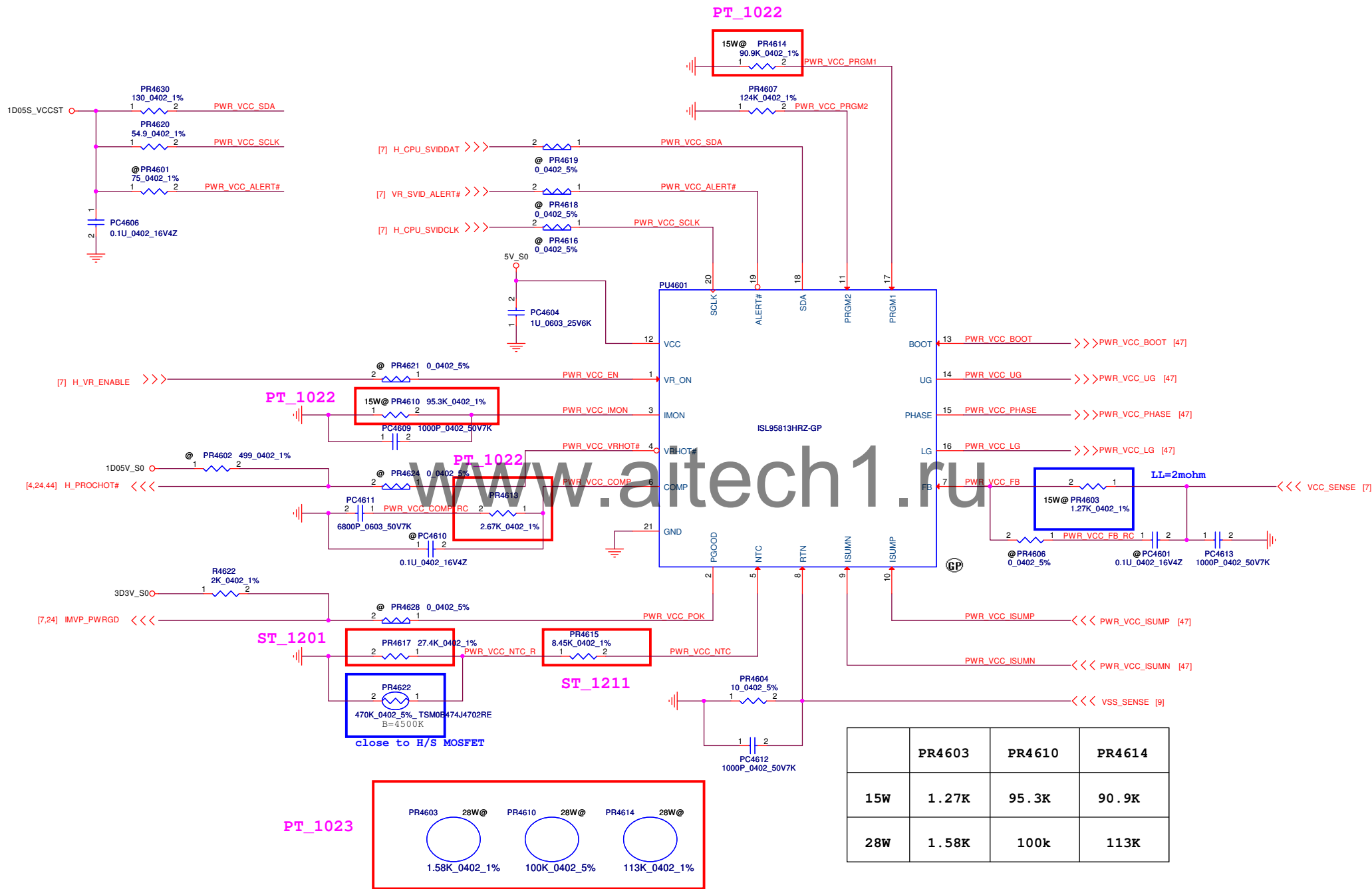


Placement: Close to Batt Connector



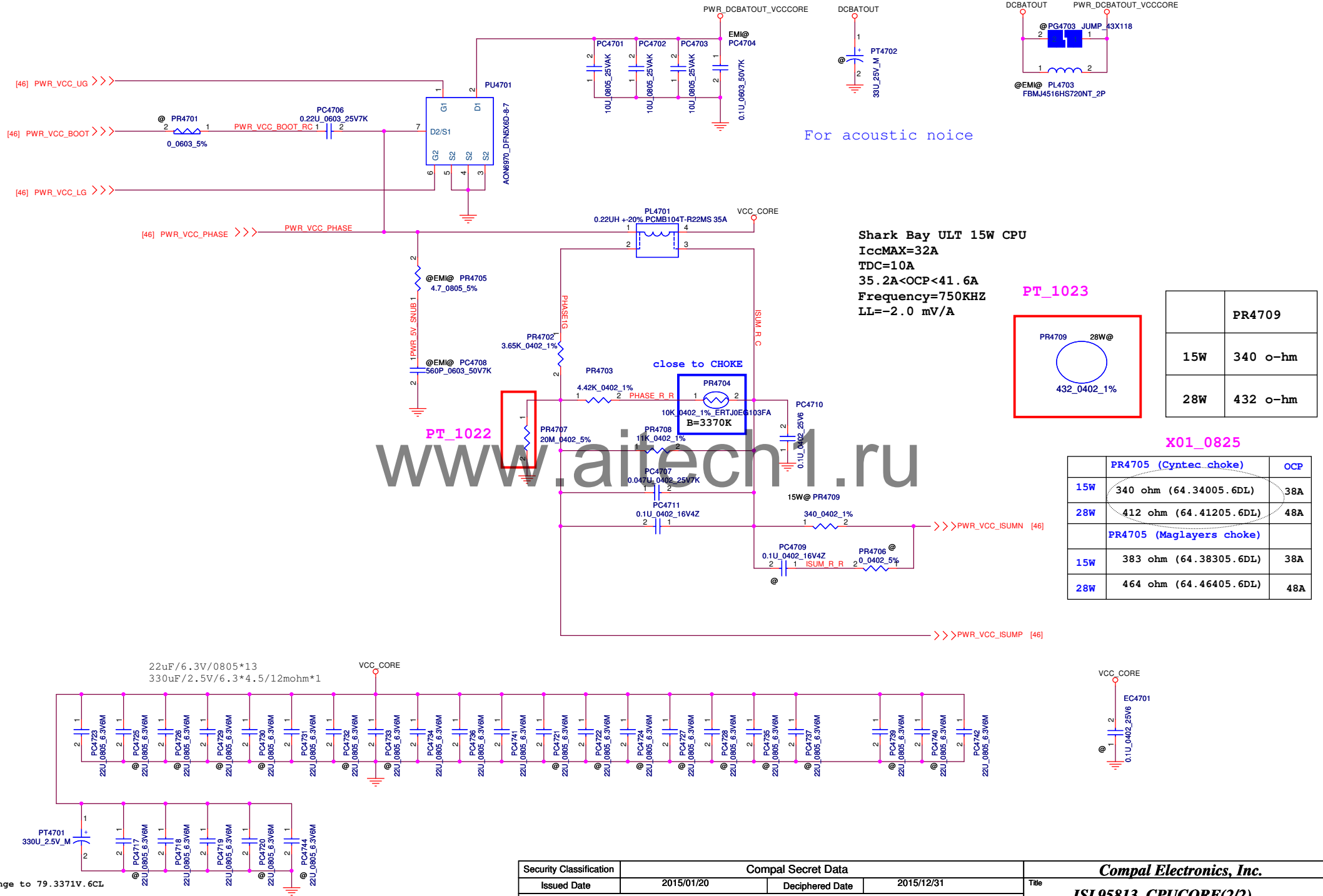
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title BATT CONN	
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Main Func = CPU_CORE

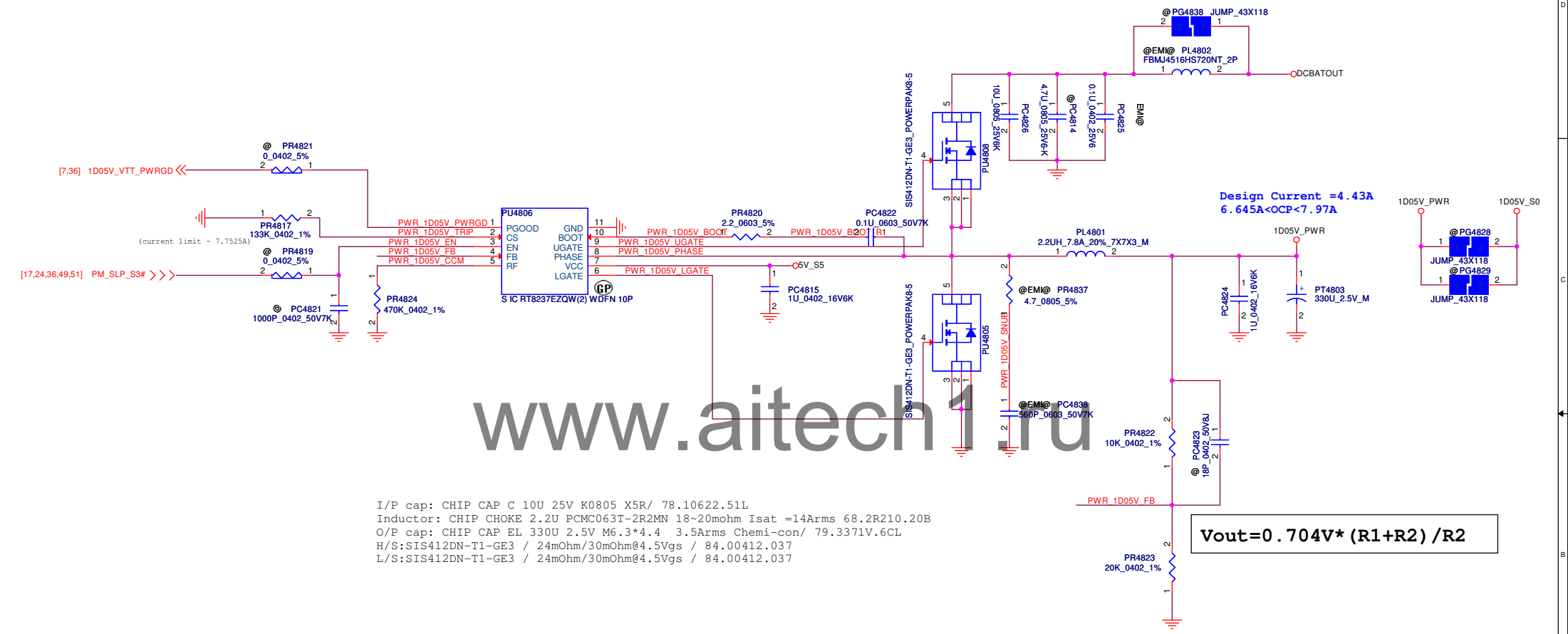


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Main Func = CPU_CORE



Main Func = 1D05V



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18~20mohm Isat =14Arms 68.2R210.20B
O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 3.5Arms Chemi-con/ 79.3371V.6CL
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

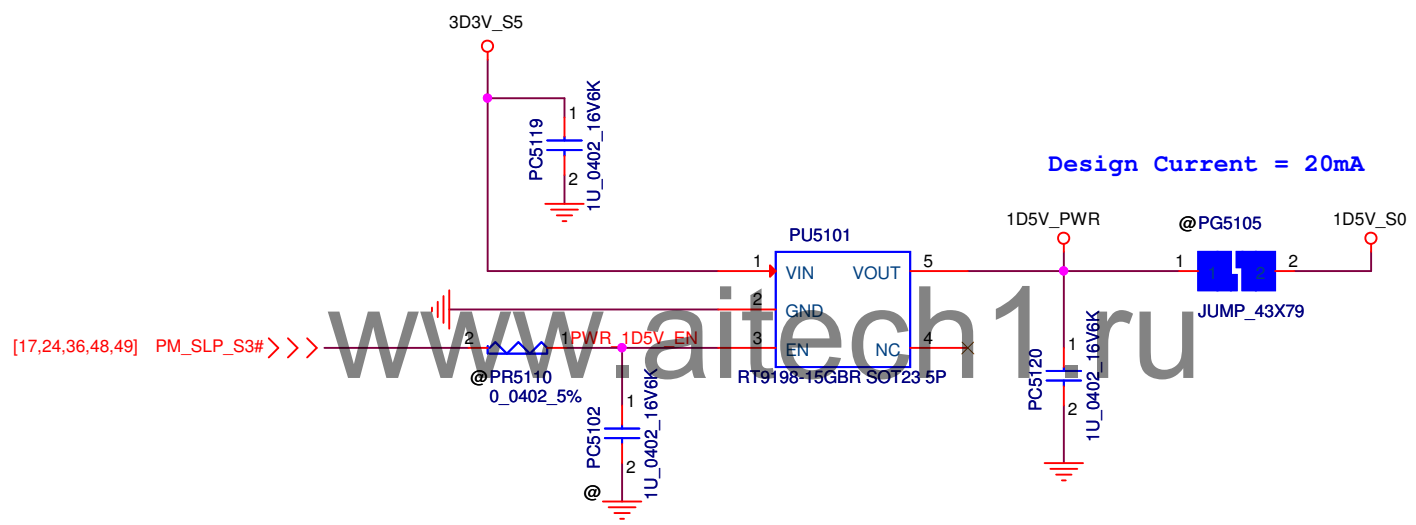
$$V_{out} = 0.704V * (R1 + R2) / R2$$

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Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title	RT8237 1D05V
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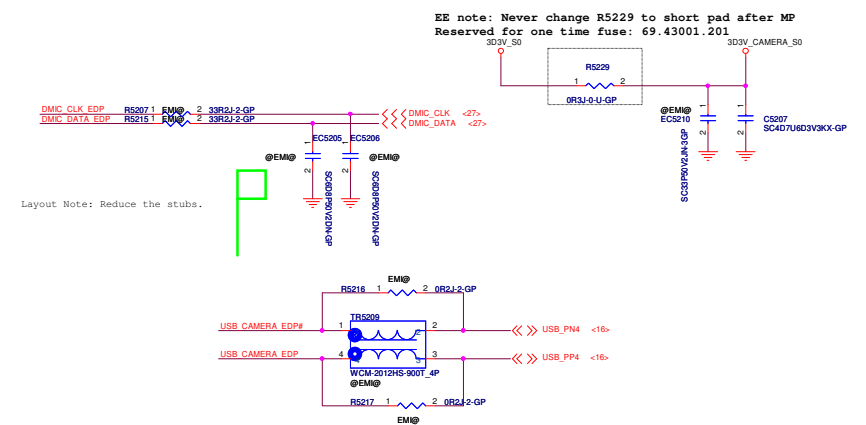
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Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title	Reserved	
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Main Func = 1D5V

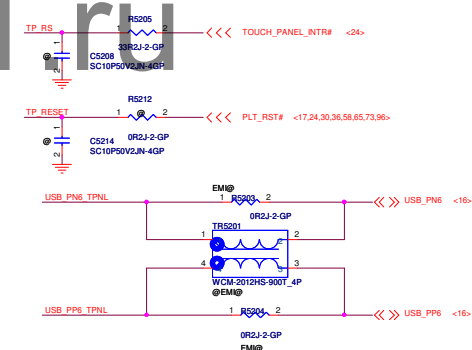


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				Document Number	Rev	
				LA-B483P	A00	
				Date:	Wednesday, January 21, 2015	Sheet 51 of 102

Main Func = CAM



Touch Panel

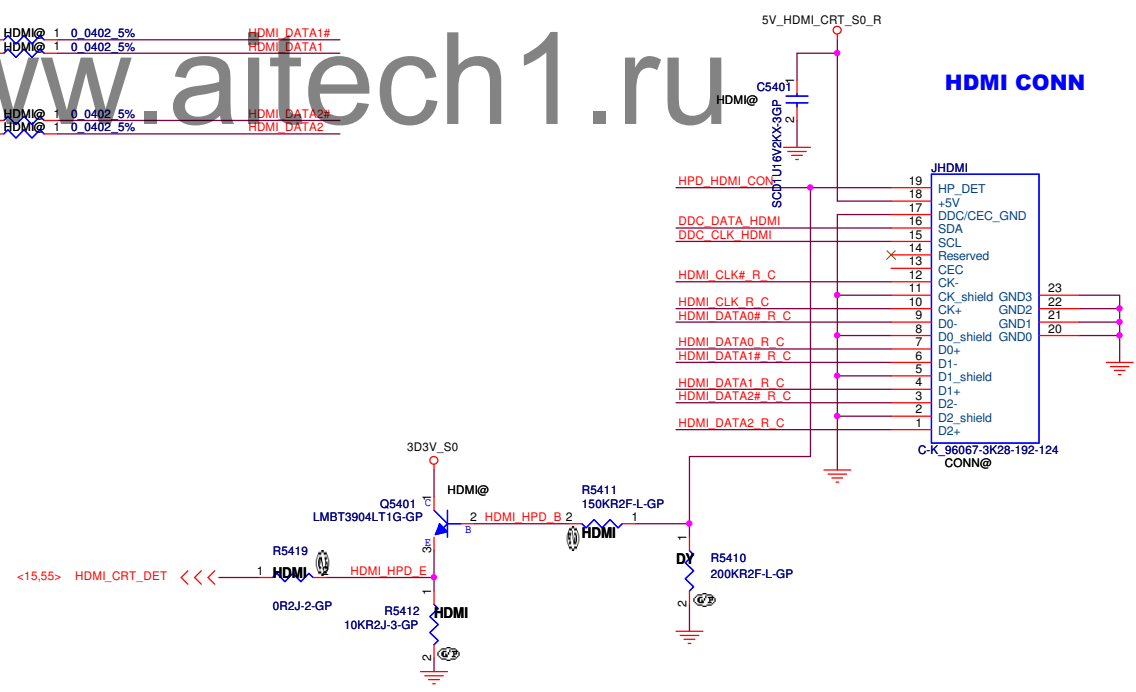
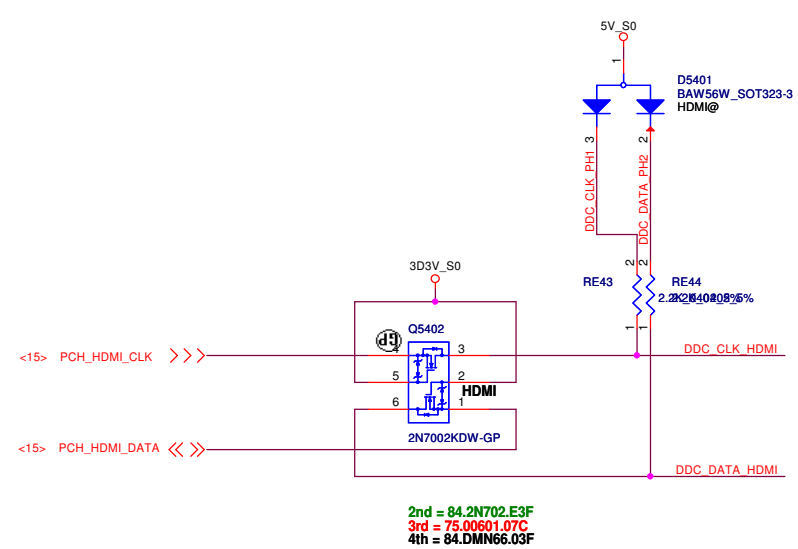
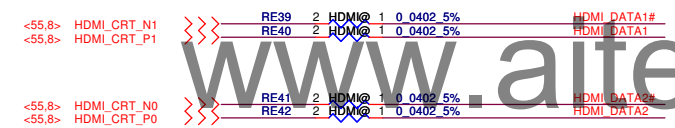
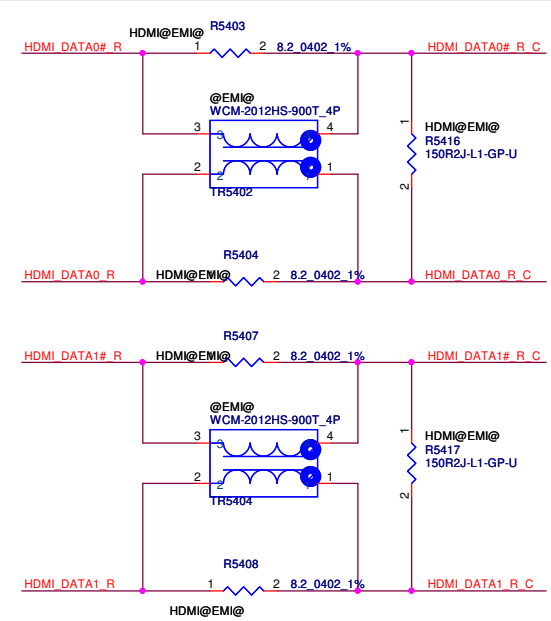
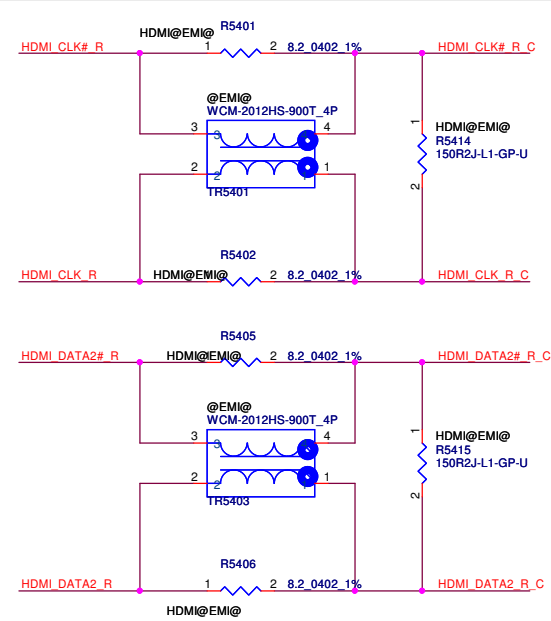
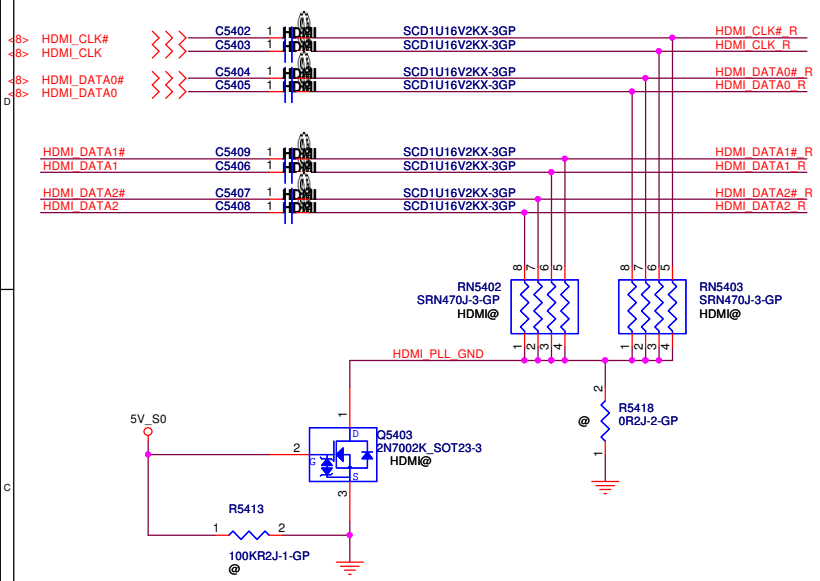


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				Sheet	53 of 102
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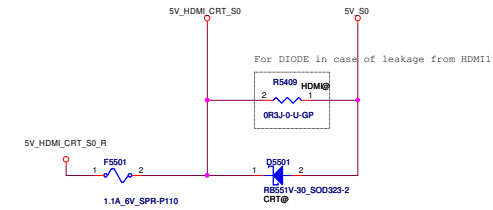
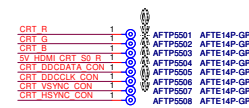
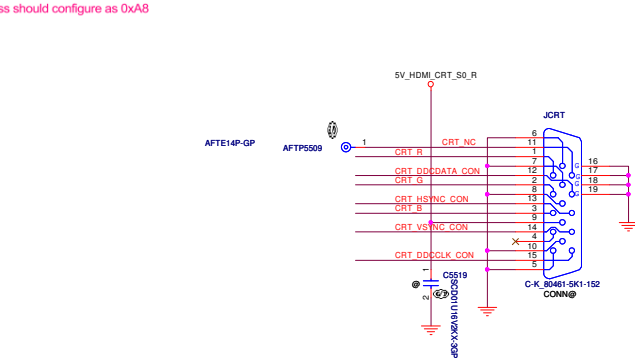
Main Func = HDMI



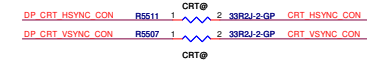
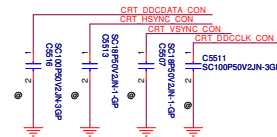
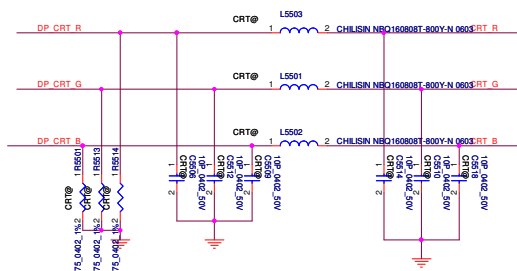
2nd = 84.2N702.E3F
3rd = 75.00601.07C
4th = 84.DMN66.03F

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				Document Number				Rev			
				LA-B483P				A00			
				Date				Wednesday, January 21, 2015			
				Sheet				54 of 102			

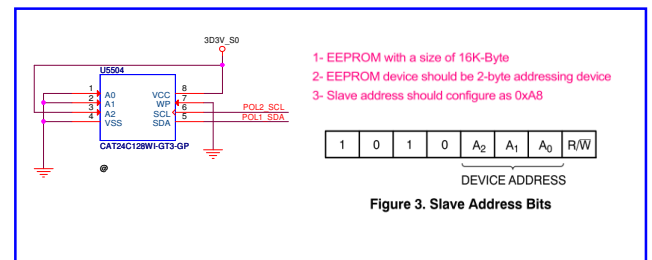
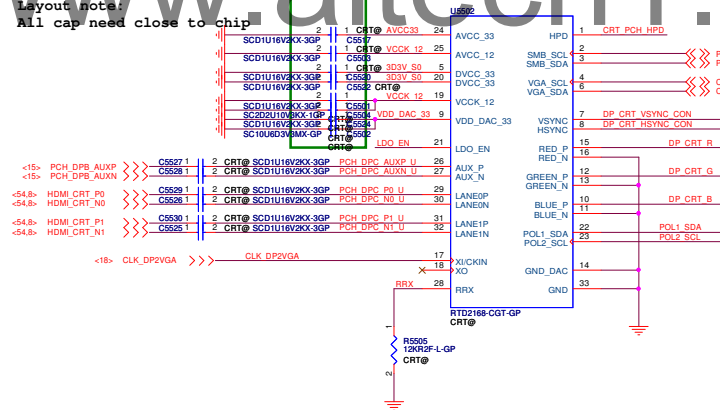
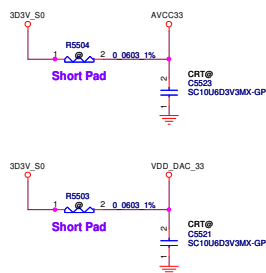
- 1- EEPROM with a size of 16K-Byte
- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8



CRT RGB
CRT H/VSYNC
CRT SMBUS



Layout note:
All cap need close to chip



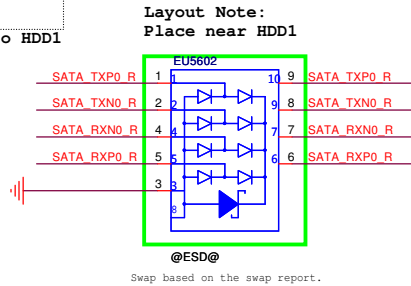
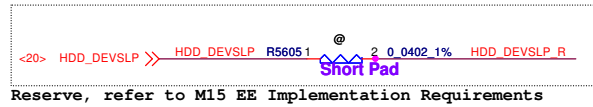
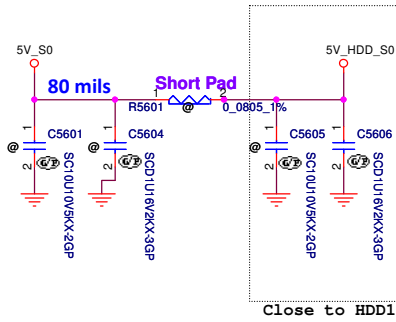
		POL1_SD4(PIN22)	
		0	1
POL2_SQ4(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V/	VCCK_V12 from Embedded LDO

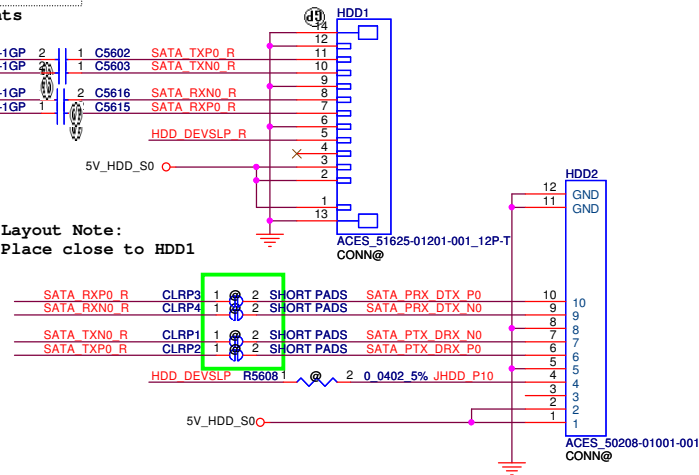
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Main Func = HDD

SATA HDD Connector



Layout Note:
Place close to HDD1

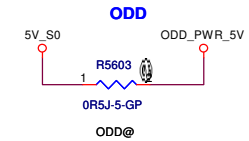
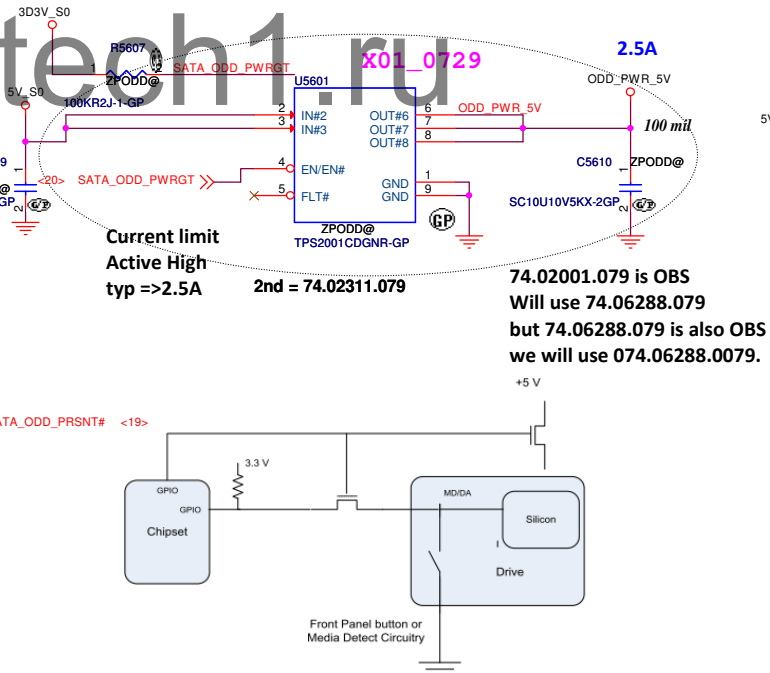
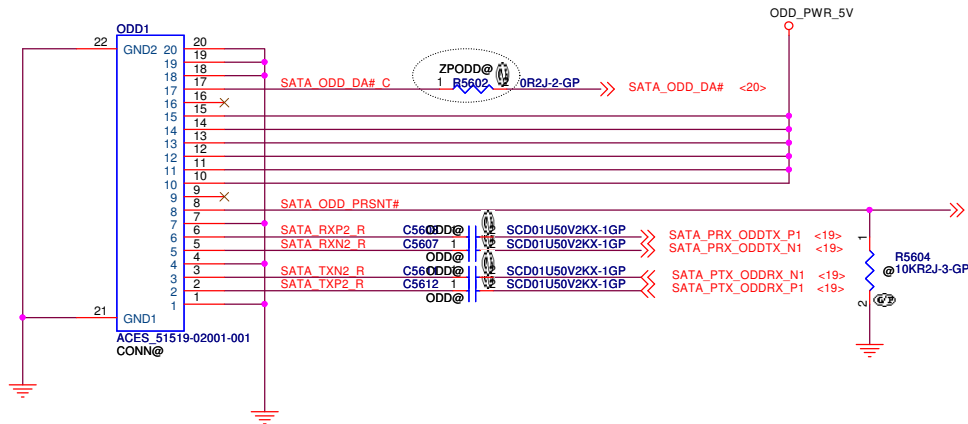


CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

Main Func = ODD

SATA Zero Power ODD

ODD Connector



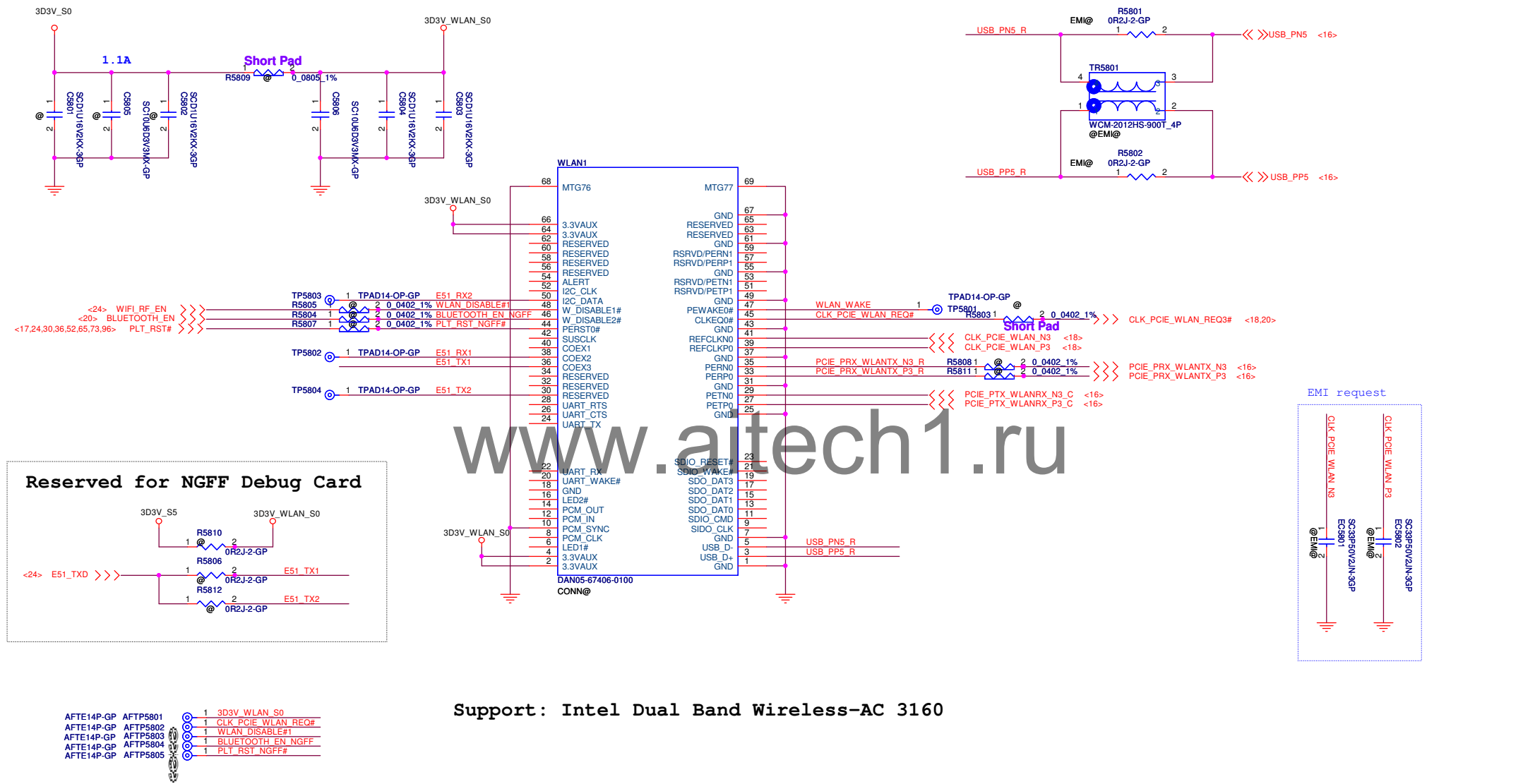
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Issued Date	2015/01/20	Deciphered Date	2015/12/31	Title	HDD/ODD
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SSID = ESATA

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Main Func = WLAN



Support: Intel Dual Band Wireless-AC 3160

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Main Func = IO Connector

I/O Board Connector

X01_0808

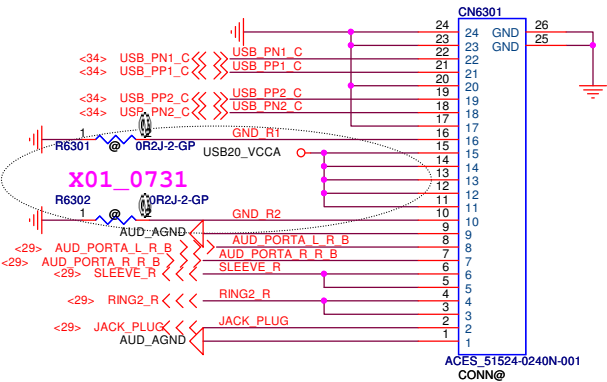
USB2 (USB2.0)

USB3 (USB2.0)

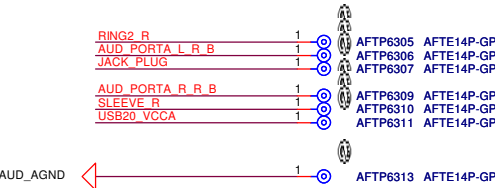
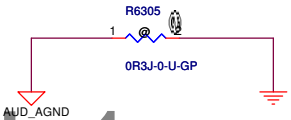
USB2 (USB2.0)

USB3 (USB2.0)

Universal Jack



Pitch: 1mm
Power: 5 pins
GND: 4 pins
AGND: 2 Pins



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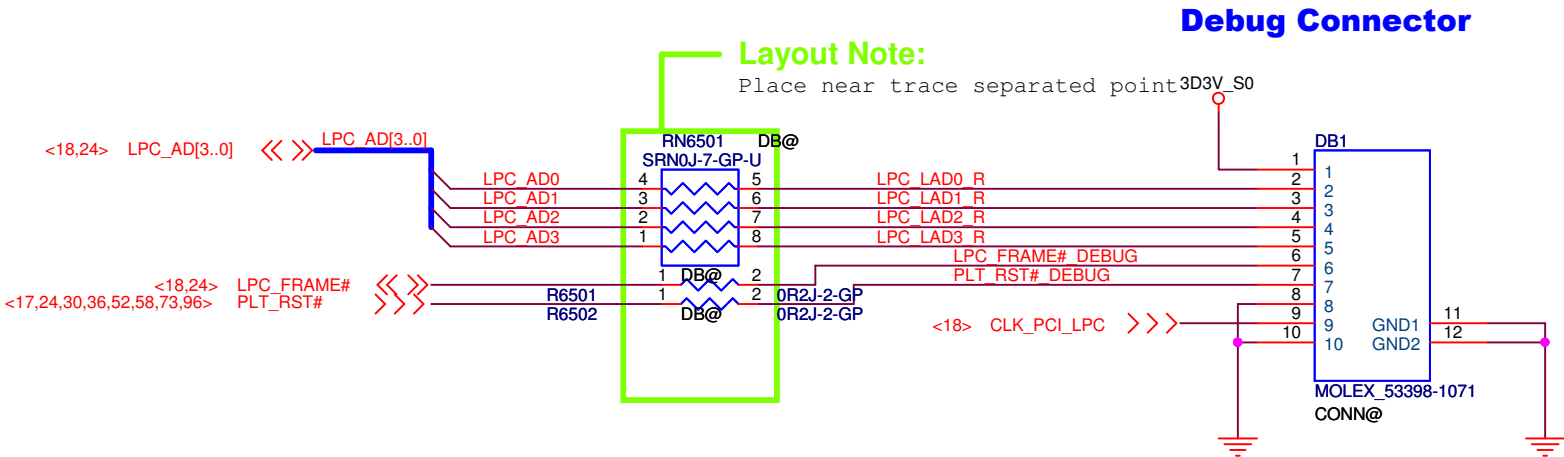
Main Func = Hall Sensor

Move to Power Button Board

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Main Func = Debug



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

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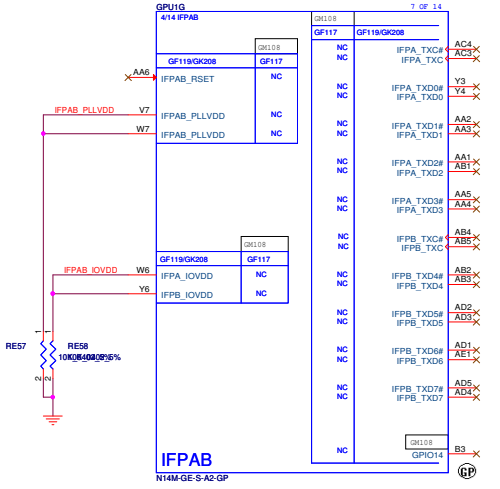
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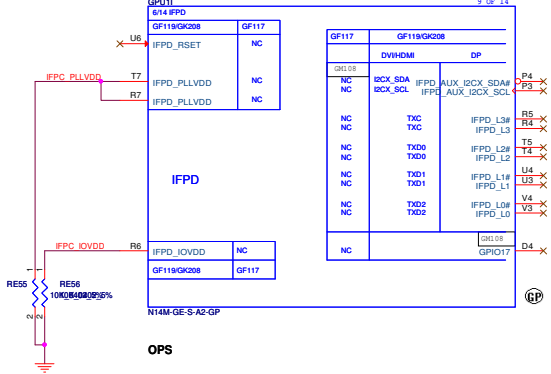
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LVDS Interface

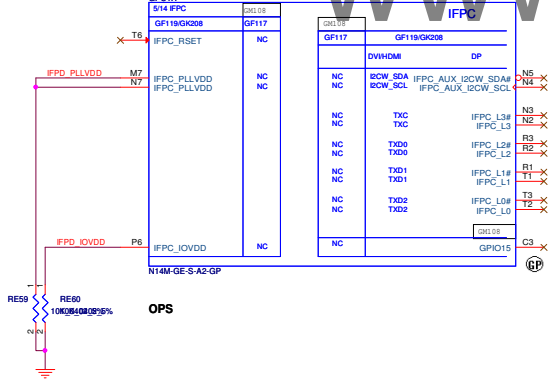


OPS

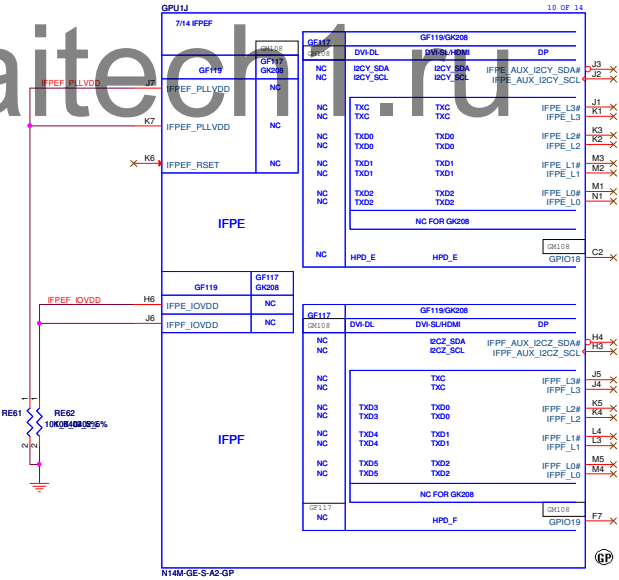


OPS

HDMI Interface



OPS



OPS

Table 3-9. DDR3 GPU-side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type	Footprint	Population	Location	
GB2B-64 DDR3	0.1 μ F	X7R 0402	2	2	Under GPU
	1 μ F	X7R 0603	2	2	Under GPU
	4.7 μ F	X6S 0603	2	2	Under GPU
	10 μ F	X5R 0805	1	1	Near GPU
	22 μ F	X5R 0805	1	1	Near GPU
GB4B-128 DDR3	0.1 μ F	X7R 0402	4	4	Under GPU
	1 μ F	X7R 0603	4	4	Under GPU
	4.7 μ F	X6S 0603	4	4	Under GPU
	10 μ F	X5R 0805	2	2	Near GPU
	22 μ F	X5R 0805	2	2	Near GPU

- Notes:**
1. The decoupling in this table applies to both single rank and dual rank designs.
 2. If a single partition 64-bit GPU in the GB4B-128 package is used, populate only half of the recommended number of decoupling capacitors of GB4B-128.

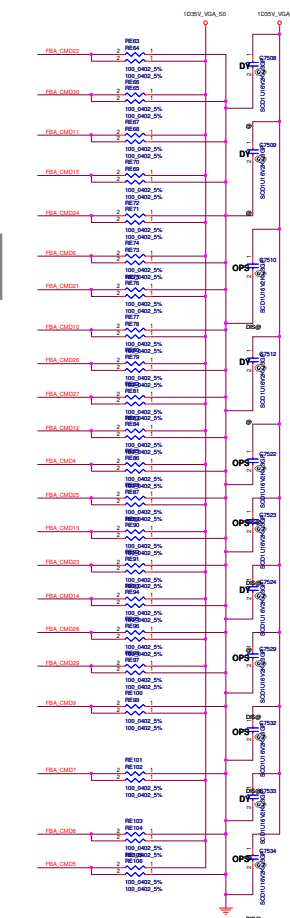
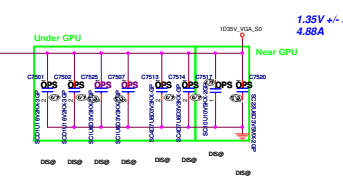
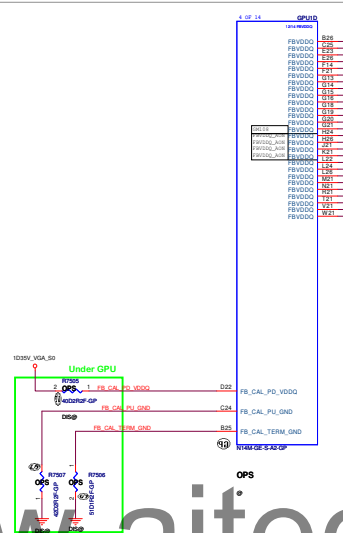
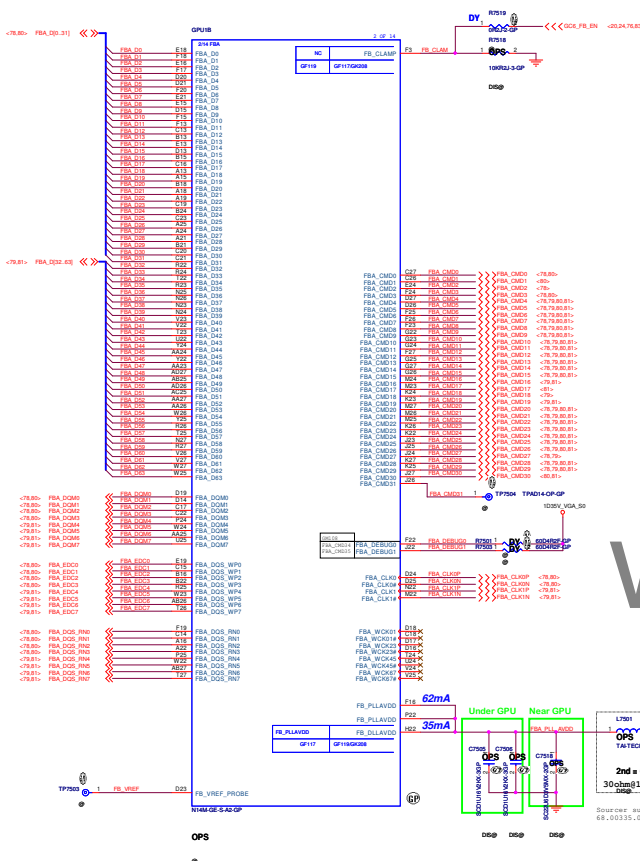


Table 6-4. Mode E Command Mapping

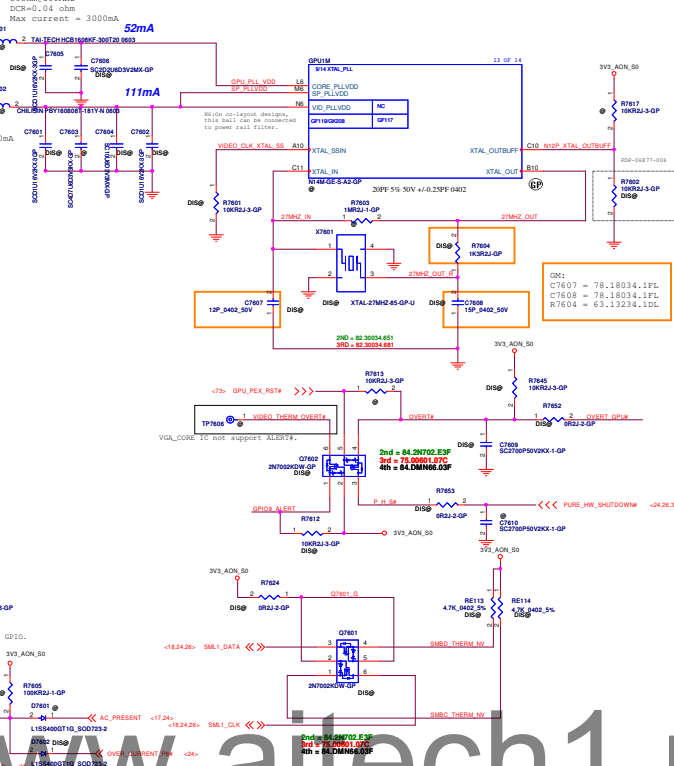
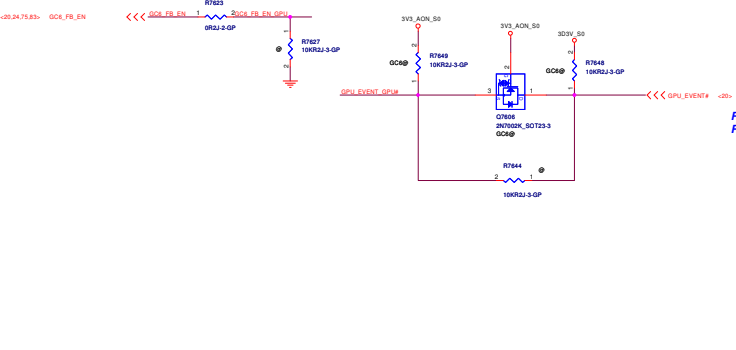
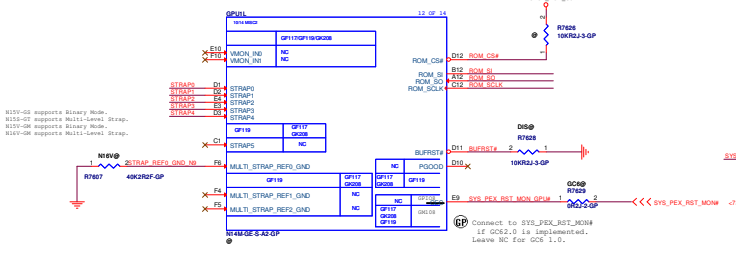
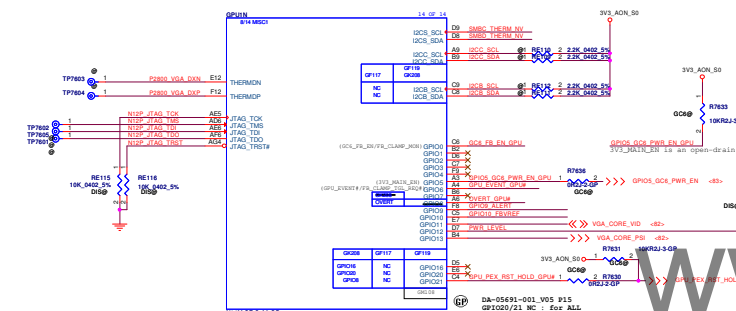
N15x DDR3 Mode E	Rank 0		Rank 1	
	Data Bits [3:0]	Data Bits [63:32]	Data Bits [3:0]	Data Bits [63:32]
FBx_CM0	ODT		ODT	
FBx_CM1			CS1*	
FBx_CM2	CS0*			
FBx_CM3	CKE		CKE	
FBx_CM4	A9	A9	A11	A11
FBx_CM5	A6	A6	A7	A7
FBx_CM6	A3	A3	BA1	BA1
FBx_CM7	A0	A0	A12	A12
FBx_CM8	A8	A8	A8	A8
FBx_CM9	A12	A12	A0	A0
FBx_CM10	A1	A1	A2	A2
FBx_CM11	RA5*	RA5*	BA5*	BA5*
FBx_CM12	A13	A13	A14	A14
FBx_CM13	BA1	BA1	A3	A3
FBx_CM14	A14	A14	A13	A13
FBx_CM15	CAS*	CAS*	CAS*	CAS*
FBx_CM16		ODT		ODT
FBx_CM17				CS1*
FBx_CM18		CS0*		
FBx_CM19		CKE		CKE
FBx_CM20	RS†	RS†	RS†	RS†
FBx_CM21	A7	A7	A6	A6
FBx_CM22	A4	A4	A5	A5
FBx_CM23	A11	A11	A9	A9
FBx_CM24	A2	A2	A1	A1
FBx_CM25	A10	A10	WE*	WE*
FBx_CM26	A5	A5	A4	A4
FBx_CM27	BA2	BA2		
FBx_CM28	WE*	WE*	A10	A10
FBx_CM29	BA0	BA0	BA0	BA0
FBx_CM30			BA2	BA2
FBx_CM31				
FBx_CM32				
FBx_CM33†				

Table 3-9. DDR3 GPU-side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type	Footprint	Population	Location	
GB2B-64 DDR3	0.1 μ F	X7R 0402	2	2	Under GPU
	1 μ F	X7R 0603	2	2	Under GPU
	4.7 μ F	X6S 0603	2	2	Under GPU
	10 μ F	X5R 0805	1	1	Near GPU
	22 μ F	X5R 0805	1	1	Near GPU

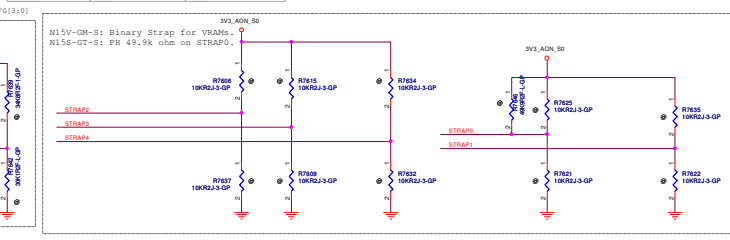
GPU Package	PLL Rail	Capacitor Type		Footprint	Population	Location
GB2B-64 and GB4B-128	PLLVD	0.1 μ F	X7R	0402	1	Under GPU
		22 μ F	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (E5R=0.05)	0402	1	Near GPU	

GPU Package	PLL Rails	Capacitor Type	Footprint	Population	Location
GB2B-64	SP_PLLVDD +	0.1 μ F X7R	0603	1 per ball	Under GPU
GB4B-128	VID_PLLVDD	4.7 μ F X5R	0603	1	Near GPU
GB3-256		22 μ F X5R	0805	1	Near GPU
Bead Type					
		180 Ω (ESR=0.2)	0603	1	Near GPU



		Strap	
128Mx16 DDR3L	Hynix	0x9	H5TC2G63FFR-11C
	Micron	0xA	MT41J128M16JT-093G:K
	Samsung	0xB	K4W2G1646E-BY11
256Mx16 DDR3L (4 pcs VRAM)	Hynix	0x3	H5TC4G63AFR-11C
	Micron	0x4	MT41J256M16HA-093G:E
	Samsung	0x5	K4W4G1646D-BC1A
256Mx16 DDR3L (8 pcs VRAM)	Hynix	0xC	H5TC4G63AFR-11C
	Micron	0xD	MT41J256M16HA-093G:E
	Samsung	0xE	K4W4G1646D-BC1A

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	0000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111



Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10kΩ	Pull-down to GND
ROM_SI	SUB_VENDTOR	10kΩ	+Pull-up to 3V3 if VBIOS ROM exists +Pull-down to GND if no VBIOS ROM
ROM_S0	VGA_DEVICE	10kΩ	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10kΩ	See note below
STRAP1	RAM_CFG[1]	10kΩ	See note below
STRAP2	RAM_CFG[2]	10kΩ	See note below
STRAP3	RAM_CFG[3]	10kΩ	See note below
STRAP4	PCIE_MAX_SPEED	10kΩ	Pull-down to GND

		Strap	STRAP3	STRAP2	STRAP1	STRAP0	
128Mx16 DDR3L	Hynix	0xC	H5TC2G63FFR-11C	1	1	0	0
	Micron	0x1	MT41K128M16JT-107G:K	0	0	0	1
	Samsung	0x5	K4W2G1646E-BY11	0	1	0	1
256Mx16 DDR3L	Hynix	0x4	H5TC4G63AFR-11C	0	1	0	0
	Micron	0xD	MT41K26M16HA-107G:E	1	1	0	1
	Samsung	0x9	K4W4G1646D-BC1A	1	0	0	1

Physical Strapping Pin	GPU	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	H155-GV H155-GM/-GT	PCI_DEV[4] S0R3_EXPOSED	SUB_VENDOR S0R2_EXPOSED	PCI_DEV[5] S0R1_EXPOSED	PEX_PL_LN_TERM S0R0_EXPOSED
ROM_S1	ALL GB2-64 H144 GB28-64 H115	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_S0	H155-GV	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	H155-GM/-GT H155-GV	DEVID_SEL USER[3]	PCIE_CFG USER[2]	USER[1]	USER[0]
STRAP1	H155-GM/-GT H155-GV H155-GM/-GT	Reserved (Keep pull-up and pull-down footprints and stuff 50k pull-up) 3GIO_PADCFG[3] Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)	3GIO_PADCFG[2] 3GIO_PADCFG[1]	3GIO_PADCFG[1] 3GIO_PADCFG[0]	3GIO_PADCFG[0]
STRAP2	H155-GV H155-GM/-GT	PCI_DEV[3] Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)	PCI_DEV[2] PCI_DEV[1]	PCI_DEV[1] PCI_DEV[0]	PCI_DEV[0]
STRAP3	H155-GV H155-GM/-GT	S0R3_EXPOSED Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)	S0R2_EXPOSED S0R1_EXPOSED	S0R1_EXPOSED S0R0_EXPOSED	S0R0_EXPOSED
STRAP4	H155-GV H155-GM/-GT	RESERVED Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)	PCIE_SPEED_CHA HGE_GE13	PCIE_MAX_SPEED	DP_PLL_VDD33V

	N15V-GM	N155-GT
Chip	N15V-GM	N155-GT
Device ID	0x1140	0x1341
Memory interface	sDDR3	sDDR3
Package	595 ball BGA 23x23mm	595 ball BGA 23 x 23 mm 598 ball BGA 29 x 29 mm

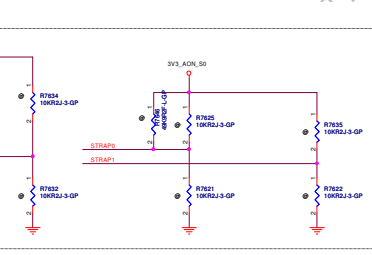


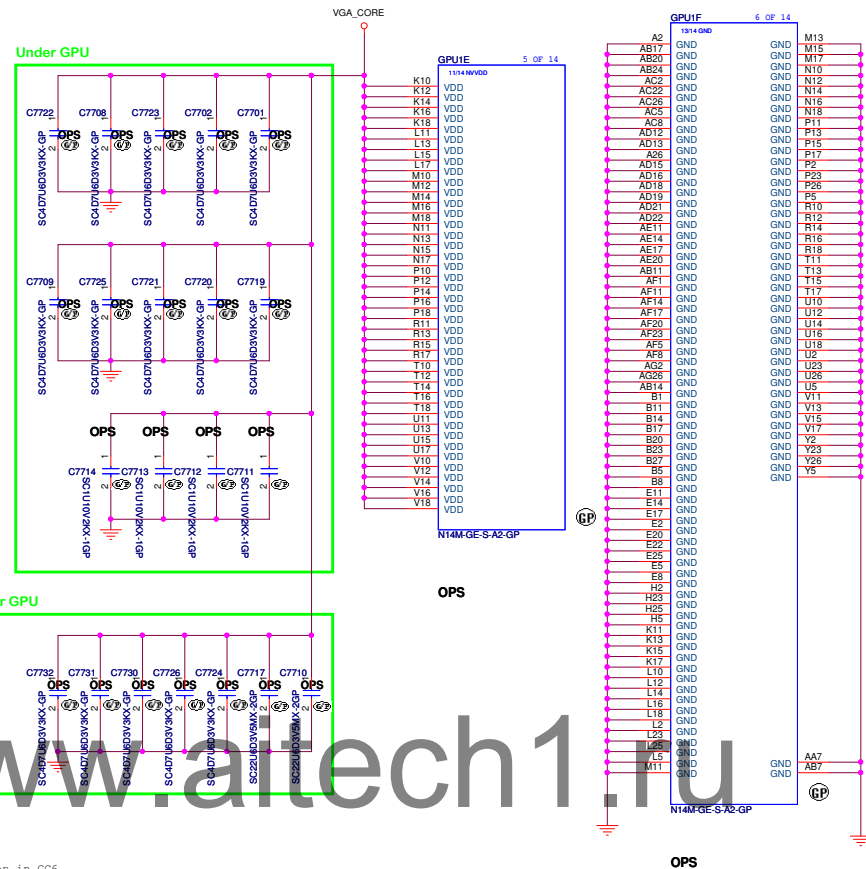
Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64	4.7 μ F	X6S	0603	10	10	Under GPU	
	1 μ F	X6S	0402	4	4	Under GPU	
	47 μ F	X5R	0805	1	1	Near GPU	
	22 μ F	X5R	0805	1	1	Near GPU	
	4.7 μ F	X5R	0805	5	5	Near GPU	
	330 μ F	POS	7343	1	1	Near GPU	ESR ≤ 6 m Ω

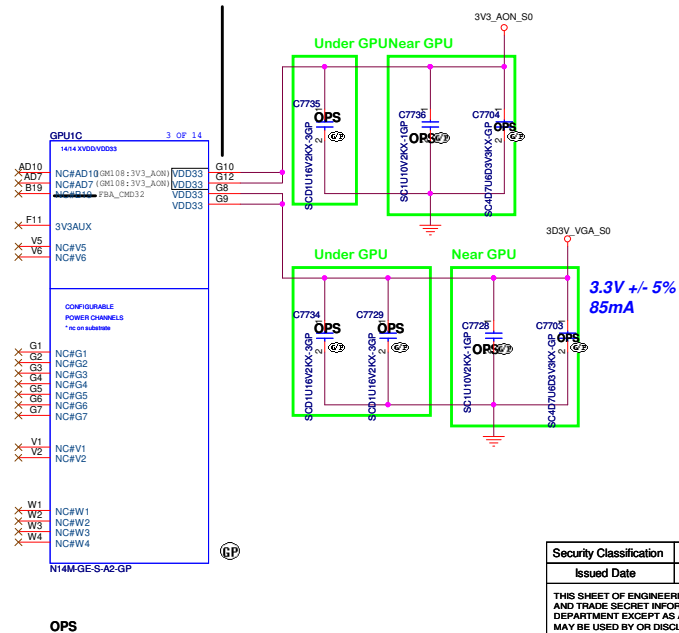
Table 3-27. 3.3V Power Rail Decoupling

GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64	3V3_MAIN	0.1 μ F	X6S	0402	2	2	Under GPU
GB4B-128		1 μ F	X5R	0603	1	1	Near GPU
GB3-256		4.7 μ F	X5R	0603	1	1	Near GPU
GB2B-64	3V3_AON	0.1 μ F	X6S	0402	1	1	Under GPU
GB4B-128		1 μ F	X5R	0603	1	1	Near GPU
GB3-256		4.7 μ F	X5R	0603	1	1	Near GPU

Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.

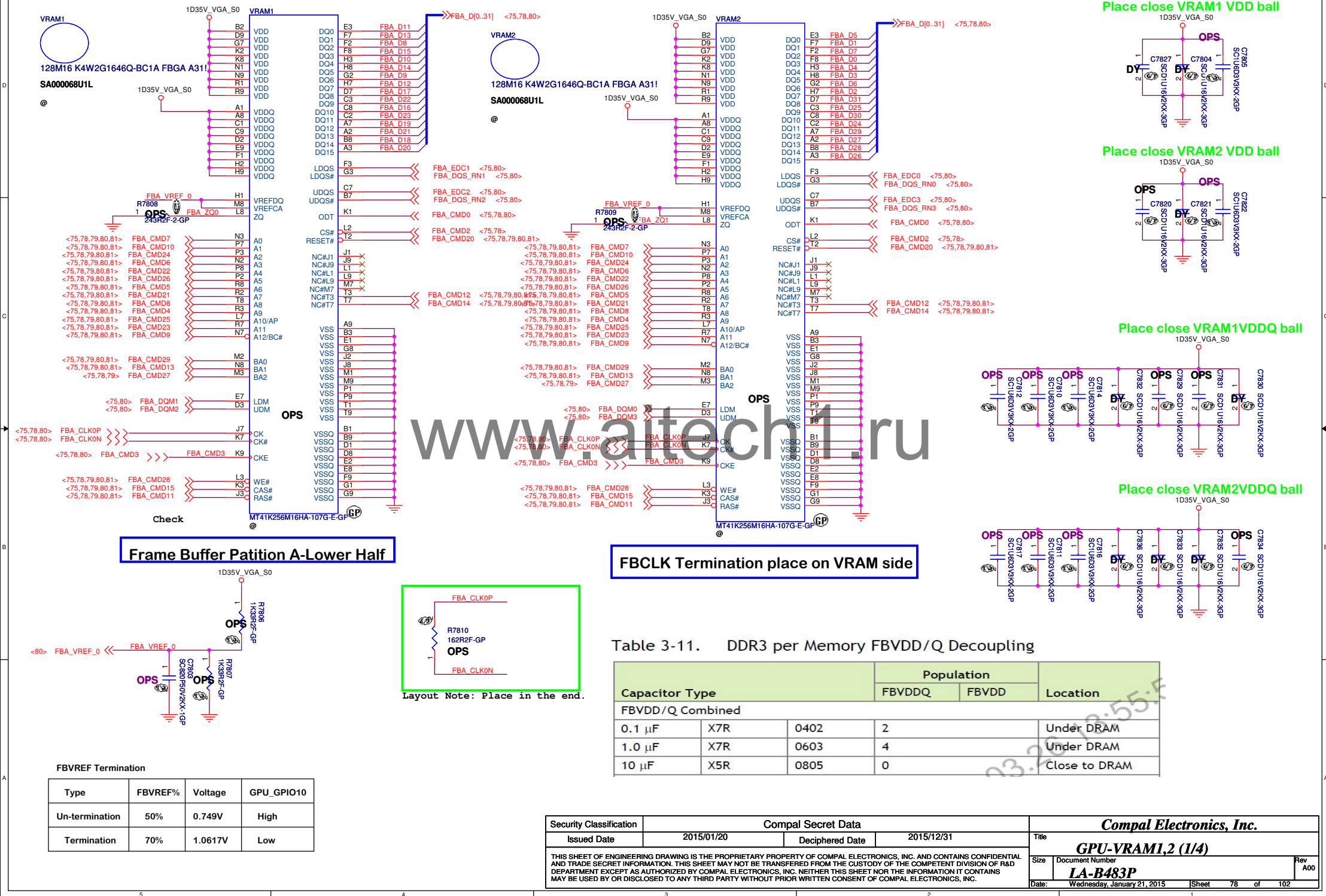


G10,G12:
If GC62.0 is implemented, connect to a 3V3 rail that will be on in GC6.
If GC62.0 is NOT implemented, connect to the same rail as VDD33.

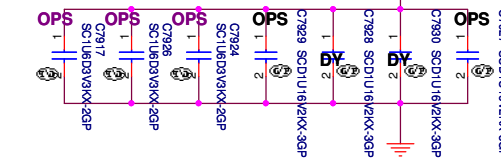


1GB, Single Rank, 4 pcs VRAM							
GPU	GPU DPN	Memory Vendor	2Gb DDR3L:(1.35v/900Mhz)	DPN	WPN	Voltage	Note
IC VGA N15V-GM-S-A2 GB2-64 FCBGA595P	JG0YH	Hynix	H5T C 2G63FR-11C	XLPRC	72.52G63.NOU	1.35V	
		Samsung	K4W2G164 E Q-BC1A	D0DP7	072.26164.0A0U	1.35V	
		Micron	MT41K128M16T-1 07 G-K	HKKF2	72.41128.NOU	1.35V	
2GB, Single Rank, 4 pcs VRAM							
GPU	GPU DPN	Memory Vendor	4Gb DDR3L:(1.35v/900Mhz)	DPN		Voltage	Note
IC VGA N15V-GM-S-A2 GB2-64 FCBGA595P	JG0YH	Hynix	H5TCA6G3A F -11C	021N2	72.05463.D0U	1.35V	Build in EV
		Samsung	K4W4G164 D -BC1A	07XGT	072.4G164.0A0U	1.35V	
		Micron	MT41K256M16H A -1 07 G-E	R5RH5	72.41K26.00U	1.35V	Build in EV
4GB, Dual Rank, 8 pcs VRAM							
GPU	GPU DPN	Memory Vendor	4Gb DDR3L:(1.35v/900Mhz)	DPN		Voltage	Note
IC VGA N15S-GT-S-A2 GB2-64 FCBGA595	FXP79	Hynix	H5TCA6G3A F -11C	021N2	72.05463.D0U	1.35V	Build in EV
		Samsung	K4W4G164 D -BC1A	07XGT	072.4G164.0A0U	1.35V	
		Micron	MT41J256M16H A - 09 3G-E	PP8P2	072.41256.0B0U	1.35V	

Data Bits 31:0 RANK 0



Data Bits 63:32 RANK 0

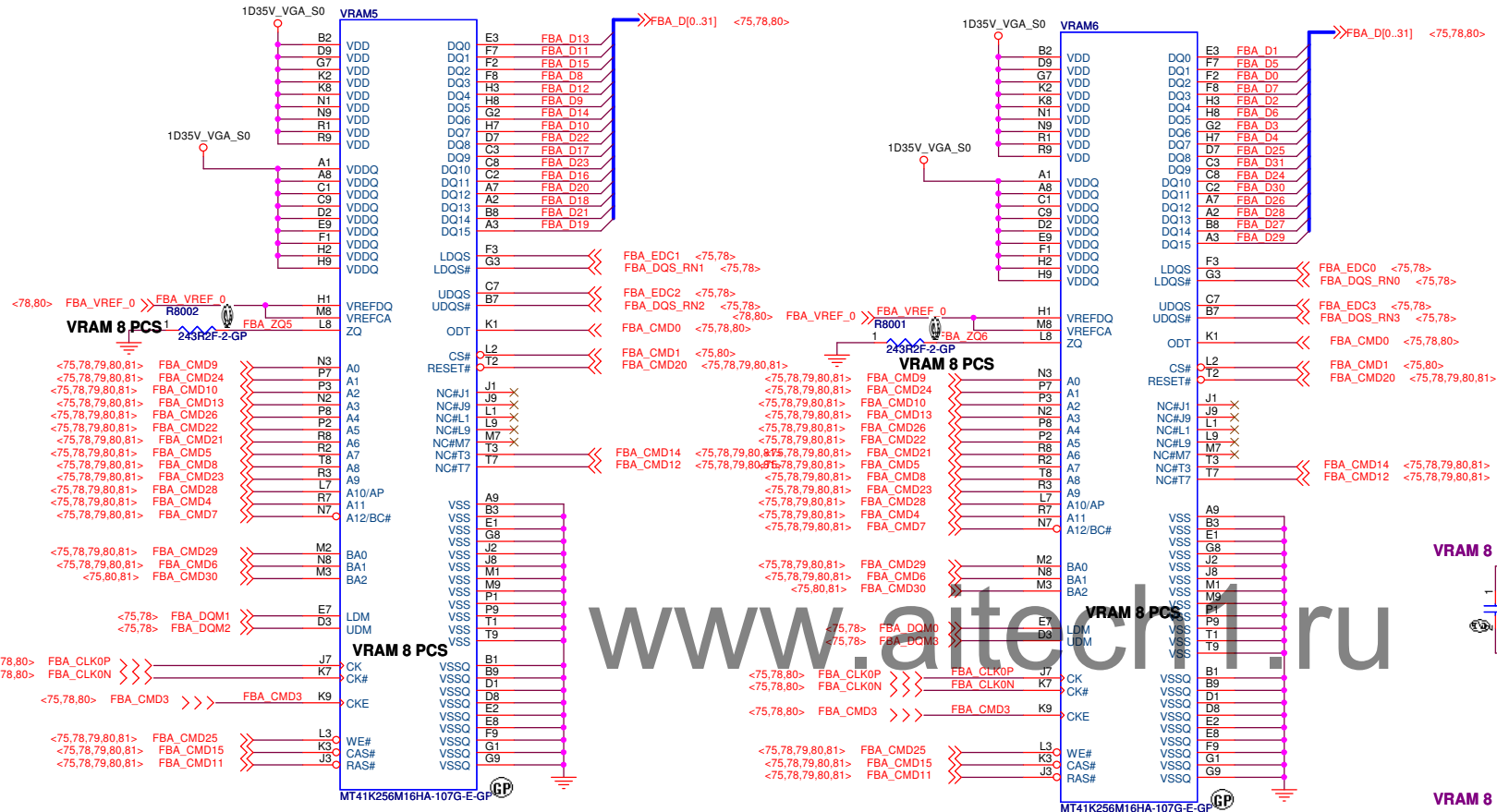


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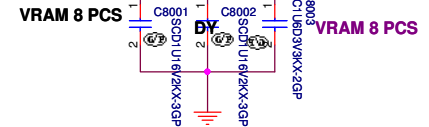
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Main Func = dGPU

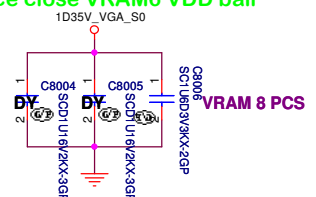
Data Bits 31:0 RANK 1



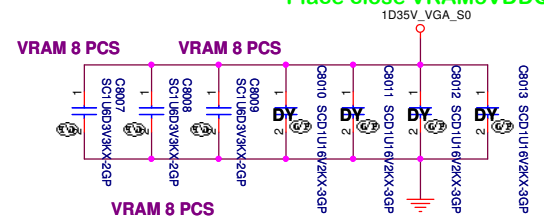
Place close VRAM5 VDD ball



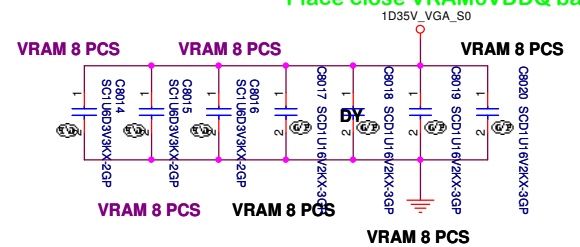
Place close VRAM6 VDD ball



Place close VRAM5VDDQ ball



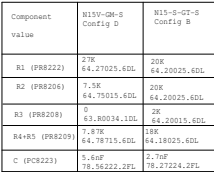
Place close VRAM6VDDQ ball



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

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78.56222.2FL:OBS REASON: 50V is more popular, chage to 78.56224.2FL

Diagram showing five circular components, each with a VGA@N16@ connection and a 20K_0402_1% resistor:

- PR8222 VGA@N16@ 20K_0402_1%
- PR8206 VGA@N16@ 20K_0402_1%
- PR8208 VGA@N16@ 2K_0402_1%
- PR8209 VGA@N16@ 18K_0402_1%
- PC8223 VGA@N16@ 2700P_0402_50V7K

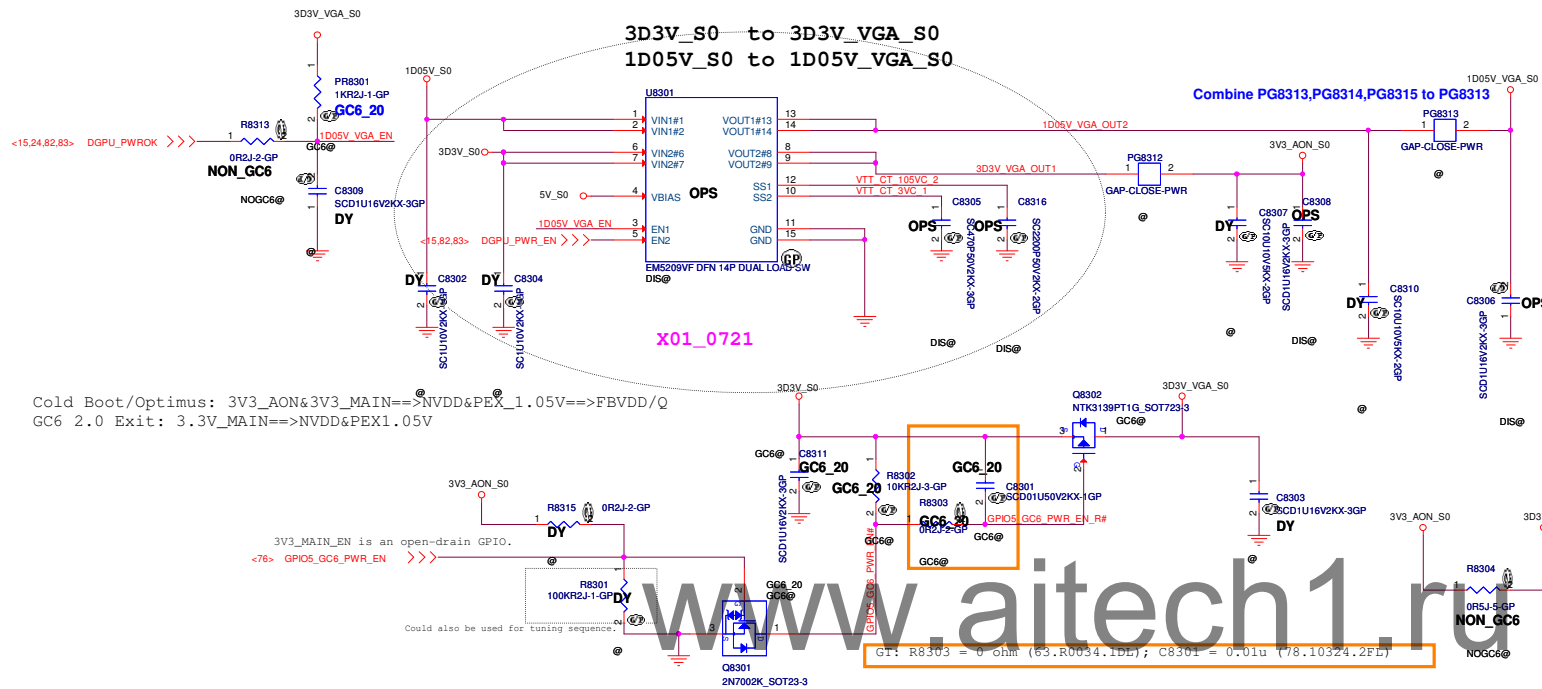
I/P capacitor: 10U 25V K05 X5R/ 78.10622.51L
 Inductor:CHIP CHOKE 0.22UH PCMC104T-R22/ 1mohm/ Isat =60A rms /68.R2210.10C
 O/P capacitor: CHIP CAP EL 330U 2.5V M6.3*4.4 Chemi-con/79.3371V.6CL
 H/S: SIRA14DP-T1-GE3 / 6.8mohm/8.5mohm@4.5Vgs/ 84.A14DP.037
 L/S:SIRA06DP-T1-GE3 / 2.75mohm/3.5mohm@4.5Vgs/ 84.SRA06.037

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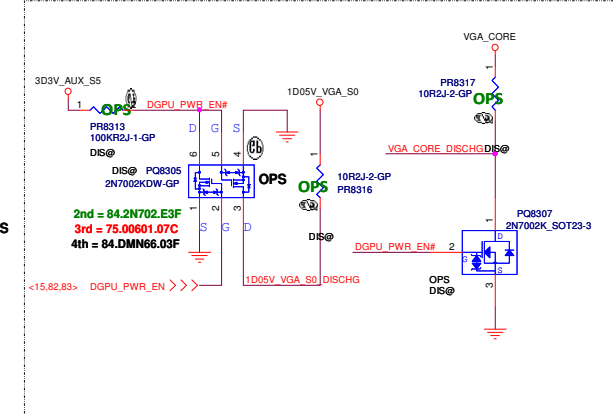
Main Func = dGPU

3D3V_VGA_S0
1D05V_VGA_S0

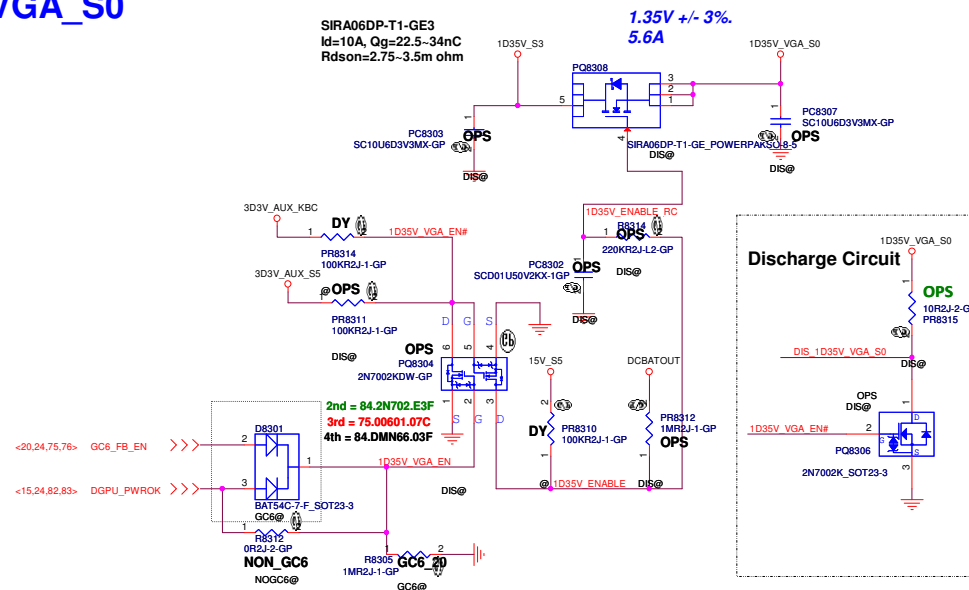
```
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D35V_VGA_S0 should ramp-up before 1D05V_VGA_S0
```



VGA_CORE&1D05V_VGA_S0 Discharge Circuit



1D35V_VGA_S0



CTx (pF)	Rise Time (µs) 10% - 90%, COU = 0.1µF @ VIN; VOUT=0 ohm load							
	Typical values @ 25°C, 25V X7R 10% ceramic cap							
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	1V	0.8V
0	107	72	46	41	36	34	33	29
220	425	276	146	122	103	91	88	74
270	489	316	172	139	121	107	104	84
470	774	487	272	224	181	159	154	123
680	1108	708	375	317	242	221	213	168
1000	1561	1007	546	441	364	314	299	234
2200	3600	2289	1240	1019	817	681	665	539
4700	7757	5092	2674	2203	1808	1592	1516	1177
10000	15700	10310	5601	4659	3674	3401	3197	2562

Table 1. Rise time vs. CTx value

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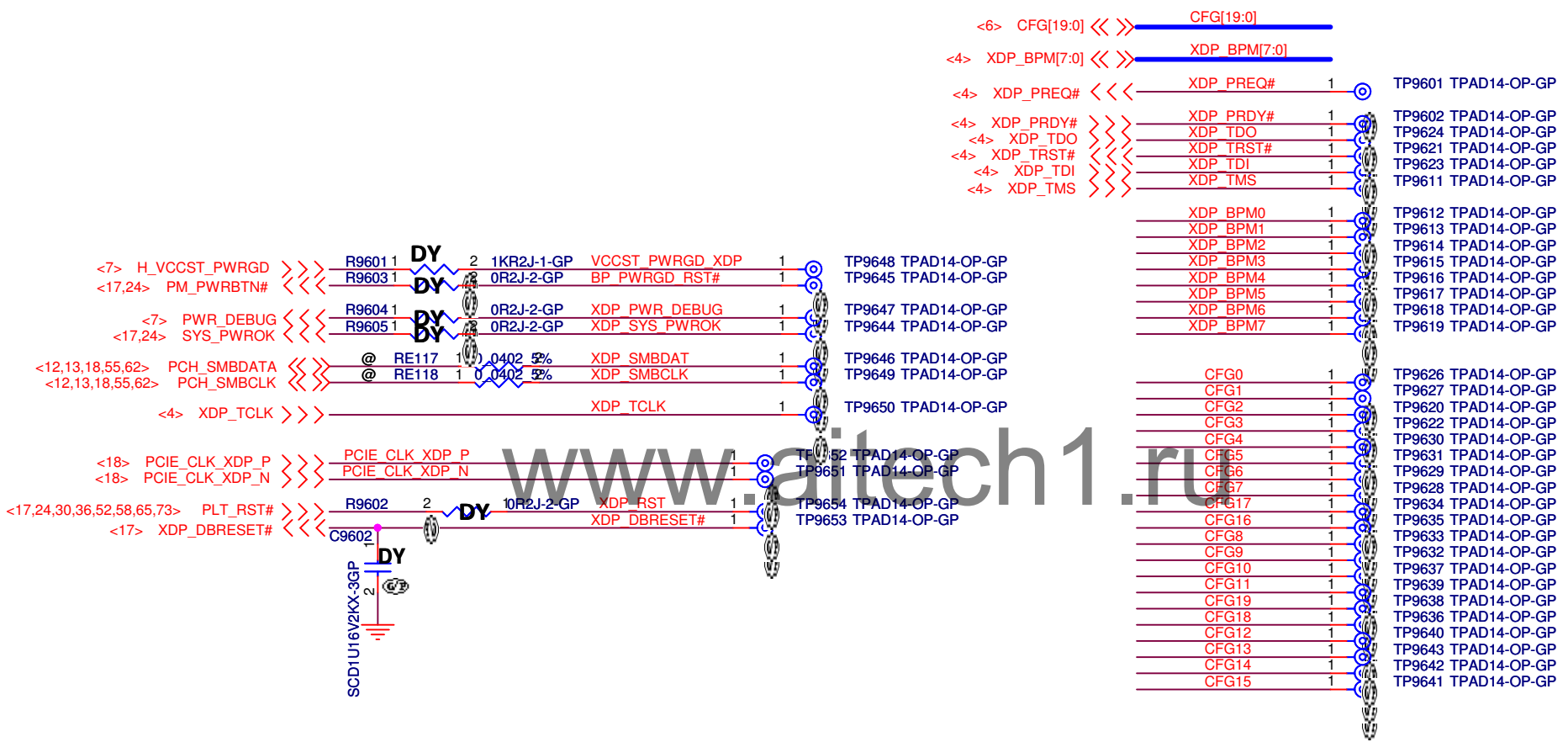
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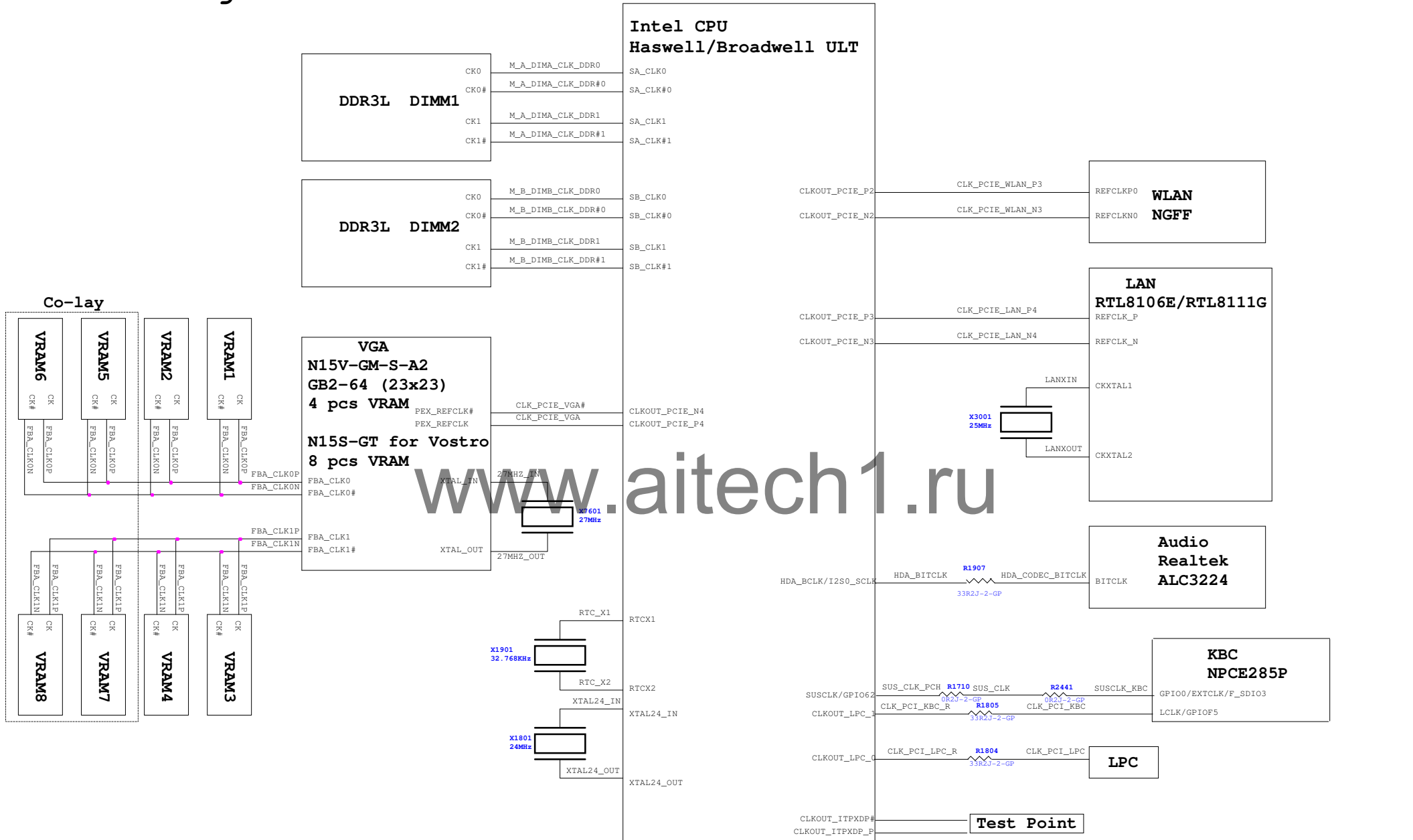
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CPU XDP



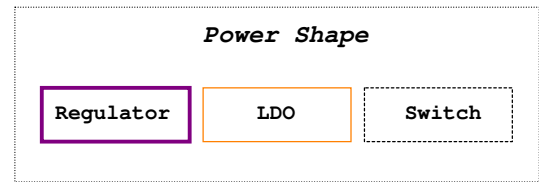
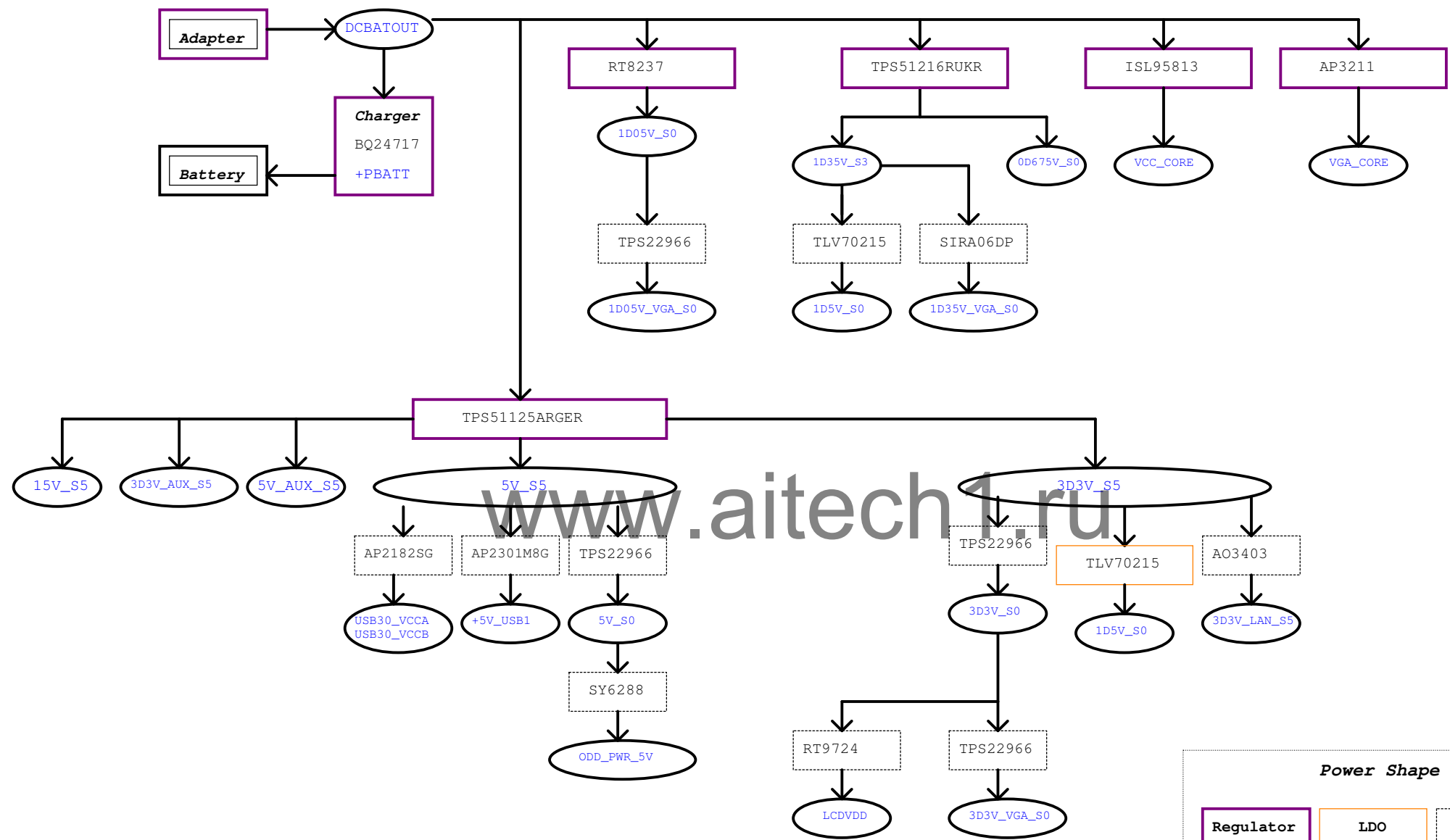
CLK Block Diagram



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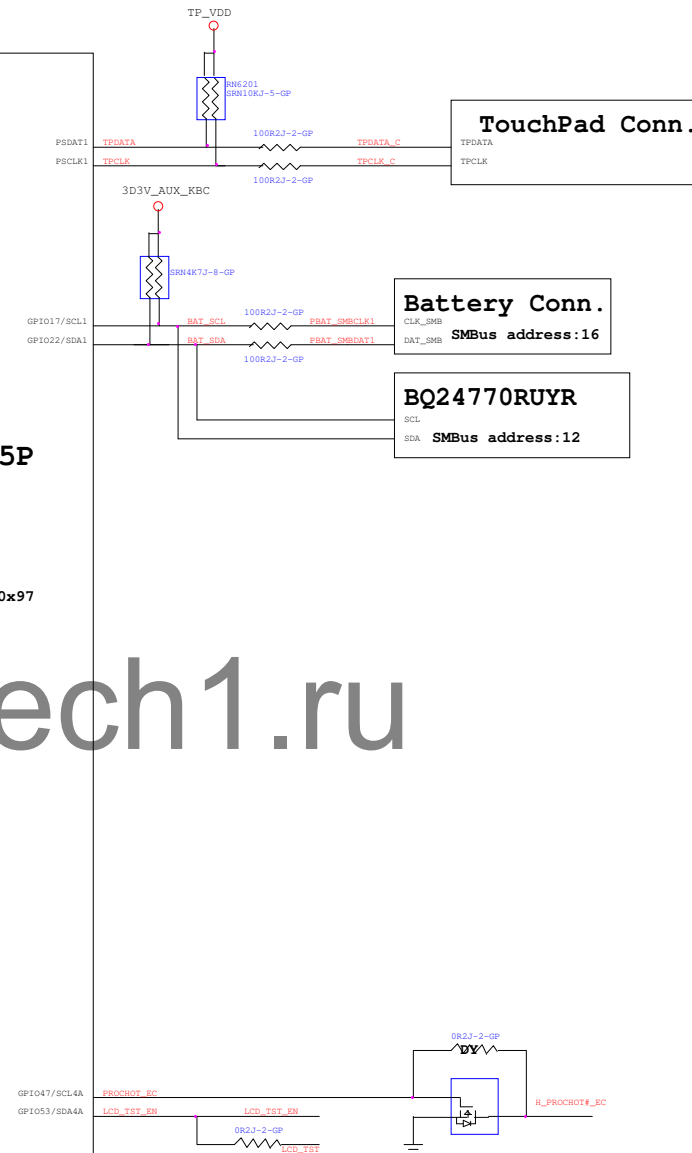
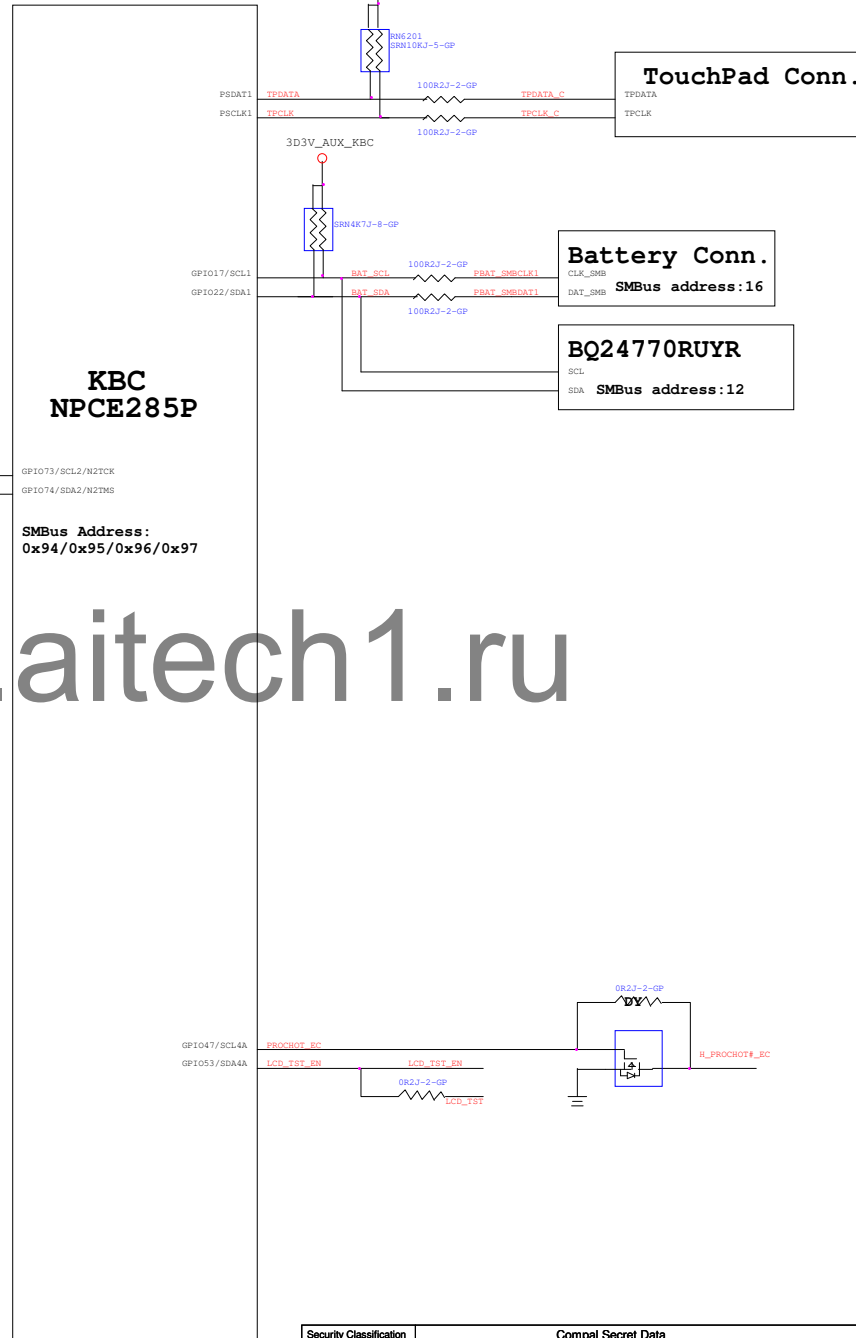
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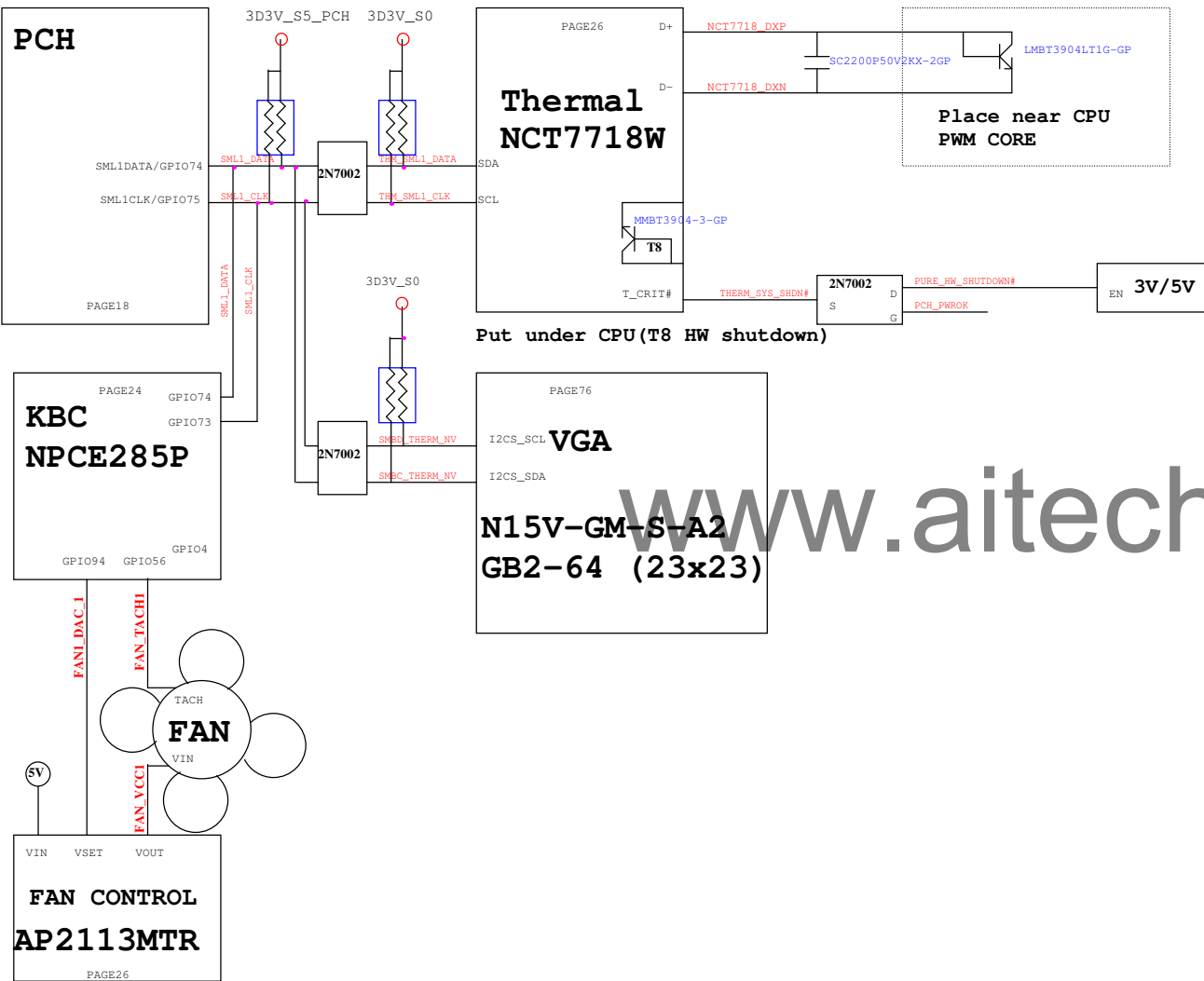
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KBC SMBus Block Diagram

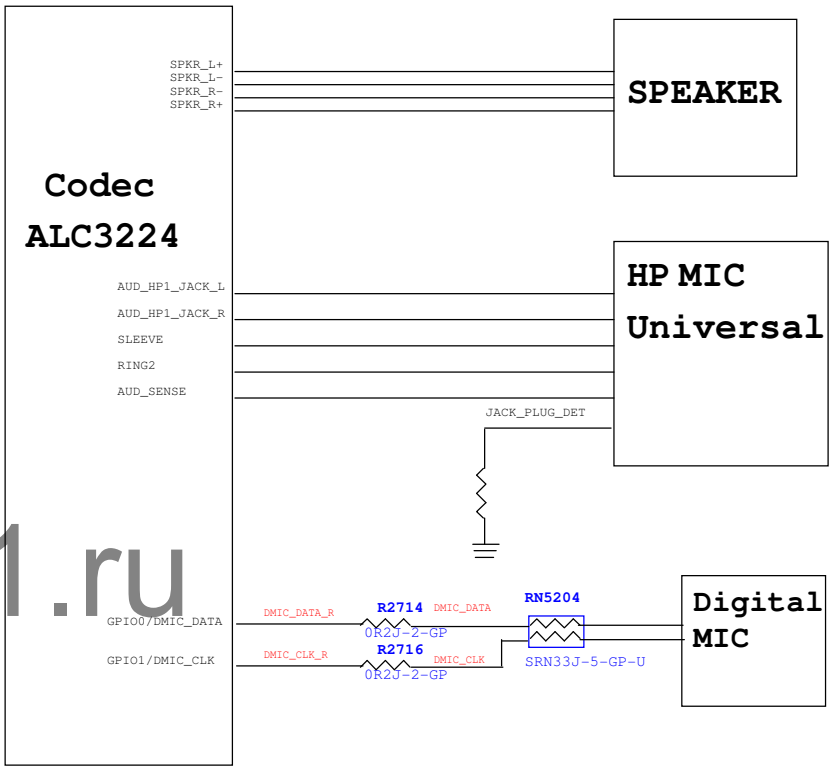


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Thermal Block Diagram



Audio Block Diagram



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